Planar Magnetics based Onboard Charger

Dissertation submitted to
Visvesvaraya National Institute of Technology, Nagpur
in partial fulfillment of requirements for the award of
the degree

Master of Technology
in
Power Electronics and Drives

by

Vrundesh Shirish Pawde (MT23PED007)

under the guidance of

Dr. Ritesh Kumar Keshri

Dr. Pratik Nachankar Mr. Milind Dighresker

Department of Electrical Engineering
Visvesvaraya National Institute of Technology
Nagpur 440 010 (India)

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Department of Electrical Engineering
Visvesvaraya National Institute of Technology, Nagpur

Declaration

I, Vrundesh Shirish Pawde hereby declare that this dissertation titled, **"Planar Magnetics Based Onboard Charger"** is carried out by me in the Department of Electrical Engineering at Visvesvaraya National Institute of Technology, Nagpur. This work is original and has not been submitted earlier whole or in part for the award of any degree/diploma at this or any other Institute or University.

VSPawde

Vrundesh Shirish Pawde
Date : 30/05/2025

Certificate

This is to certify that the dissertation titled **"Planar Magnetics Based Onboard Charger"** submitted by **Vrundesh Shirish Pawde** in partial fulfillment of the requirements for the award of the degree of **Master of Technology in Power Electronics and Drives**, VNIT Nagpur. The work is comprehensive, complete and fit for evaluation.

30/05/25

Dr. Ritesh Kumar Keshri
Associate Professor
Department of Electrical Engineering
VNIT, Nagpur, India - 440 010

PNachankar

Dr. Pratik Nachankar
Research and Engineering Scientist
ZOHO Business Services LLP, Nagpur, India

Mr. Milind Dighresker
Senior Director, Applications
ONSEMI, Bangalore, India

विद्युत अभियांत्रिकी विभाग * DEPT. OF ELECTRICAL ENGINEERING * वि.रा.प्रौ.सं., नागपुर VNIT, Nagpur

Dr. B. S. Umre
Professor & Head, Department of Electrical Engineering
VNIT, Nagpur, India - 440 010
Date : 30.05.2025

Department of Electrical Engineering
Visvesvaraya National Institute of Technology, Nagpur

NON-PLAGIARISM CERTIFICATE

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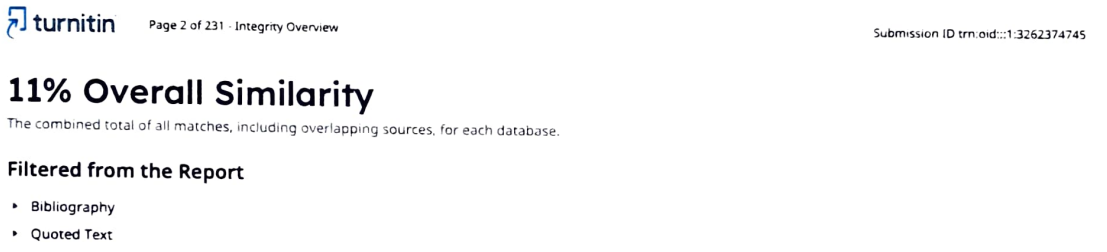
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Student ID	:	30810
Date	:	30/05/2025

R.K. Keshri 30/05/25

Dr. Ritesh Kumar Keshri
Associate Professor,
Department of Electrical Engineering,
VNIT, Nagpur

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Signature	:	VSPawde
Name	:	Vrundesh Shirish Pawde
Enrollment No.	:	MT23PED007
Student ID	:	30810
Date	:	30/05/2025

Abstract

This thesis presents a comprehensive study on the implementation and integration of planar magnetics across various subsystems of electric vehicles (EVs), with a specific focus on miniaturization, functional optimization, and system-level simplification. The research addresses three critical challenges where planar magnetic technologies can offer substantial advantages.

The first contribution focuses on eliminating the need for a dedicated auxiliary power module (APM) within EVs. This is achieved through the incorporation of a tertiary winding in a planar transformer, enabling simultaneous charging of both the main battery pack (MBP) and the auxiliary battery pack (ABP) during grid-connected charging, as well as continuous ABP charging during vehicle operation. This architecture significantly reduces component count and system complexity while enhancing power density.

The second application explores the development of a non conductive, universal charging gun based on planar magnetic coupling. This innovative design redefines conventional EV charging interfaces, offering galvanic isolation, safety improvements, and mechanical standardization across different vehicle platforms.

The third application includes the prototyping of a planar magnetics based Vehicle to Vehicle (V2V) charging connector, allowing one EV to charge another without reliance on external infrastructure paving the way for universal power sharing between two EVs.

In the biomedical domain, the thesis presents the design and realization of a 60W flyback converter integrated with a USB Power Delivery (USB PD) interface. This converter supports dynamic output voltage regulation to accommodate multiple operating modes of an ECG monitor. The system was developed, prototyped, and validated to ensure compliance with performance and safety standards required for medical-grade applications.

Finally, this work also covers the modeling and experimental validation of an advanced gate driver tailored for traction inverter applications. The developed gate driver includes key protection mechanisms such as Desaturation (DESAT), Overvoltage Clamp (OVC), Active Miller Clamping (AMC), and Programmable Soft Turn Off (PSTO). On a custom evaluation board testing and validation of the full range of protection and drive functionalities under realistic conditions is done.

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Symbols

f_s	Switching frequency
L	Inductance of the transformer or inductor
C	Capacitance
k	Coupling coefficient
N_p	Number of primary turns
N_s	Number of secondary turns
P_{loss}	Power loss
P_{in}	Input power
P_{out}	Output power
μ_r	Relative permeability of core material
A_e	Effective core cross-sectional area
l_e	Effective magnetic path length
B_{max}	Maximum flux density

List of Publications

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CHAPTER 1

Literature Review

1.1 Introduction

Planar magnetic technology represents a significant advancement in power electronics, driven by the need for compact, efficient, and reliable power conversion solutions. With the rapid growth in telecommunications, automotive electronics, aerospace, and data processing, the demand for high-density power converters has led to increased adoption of planar magnetics. Unlike conventional wire-wound magnetic components, planar magnetics utilize flat windings embedded in printed circuit boards (PCBs) along with thin, laminated magnetic cores, providing substantial advantages in terms of manufacturability, thermal management, and electrical performance [1, 2].

Historically, power electronics relied extensively on traditional transformers and inductors featuring wire-wound coils, which posed challenges in manufacturing consistency, thermal management, and miniaturization. The introduction of planar magnetic technology has addressed these issues, offering greater design flexibility, enhanced heat dissipation, and improved power density. As such, planar magnetics have become increasingly prevalent in high-frequency switching power supplies and DC-DC converters, marking a paradigm shift in magnetic component design [3, 4].

This literature review systematically examines planar magnetic technology, outlining its fundamental characteristics, detailed design considerations, challenges such as winding losses and leakage inductance, advanced structures like planar sandwiched magnetics, practical applications, and potential future research directions.

1.1.1 Fundamental Properties of Planar Magnetics

Planar magnetics have emerged as a critical innovation in the design of modern high-frequency power electronic systems. The planar structure is typically realized by integrating copper windings and dielectric layers into multilayer printed circuit boards (PCBs), enclosed within a magnetically permeable low-profile core. These designs offer considerable advantages in terms of form factor, thermal performance, and manufacturing repeatability. Unlike conventional magnetic components that use cylindrical windings, planar devices utilize flat, disk-like structures that support increased effective area relative to their volume, improving magnetic material utilization.

One of the main structural differences involves the reduction of winding window height, which consequently reduces the window area. However, this trade-off is acceptable in high-frequency designs since the full window area is rarely utilized. This configuration leads to multiple advantages, making planar magnetics favorable in compact and high-efficiency applications [5, 6].

1.1.2 Profile and Thermal Efficiency

One of the foremost benefits of planar magnetics is their reduced vertical dimension. These components inherently support low-profile configurations, facilitating integration into miniaturized systems. In general, the height of a planar magnetic device ranges between one-quarter and one-half the height of an equivalent conventional wire-wound component. This dimensional advantage simplifies system packaging and enables the use of thinner enclosure geometries, particularly beneficial in automotive, aerospace, and portable electronics sectors [7].

In addition to physical compactness, planar magnetic cores exhibit superior thermal behavior. This is primarily attributed to their higher surface area to volume ratio compared to traditional magnetic components. The increased surface facilitates enhanced

heat dissipation, leading to lower steady-state temperature rises under operational conditions [8].

To illustrate this, consider a comparative study between a conventional core and a planar core. Both cores share identical cross-sectional dimensions, volumes, and window areas. Each is paired with equivalent aluminum heat spreaders, and simulations are performed under natural convection at an ambient temperature of 30°C with a uniform power loss of 2W. Results show that the planar configuration maintains a significantly lower operating temperature, thereby affirming its thermal superiority. This performance advantage becomes particularly important in high-frequency applications, typically in the range of 100kHz to several MHz, where thermal management directly impacts system reliability and efficiency [9, 10].

1.1.3 Manufacturing Advantages

Planar magnetics are conducive to automated manufacturing processes, a key enabler for cost-effective mass production. The winding process is inherently more consistent and less labor-intensive due to the reliance on PCB fabrication techniques and computer-aided manufacturing tools. This significantly reduces production complexity, enhances throughput, and minimizes manual assembly errors.

The standardization of the fabrication process also contributes to unmatched repeatability. Each unit is produced using the same programmed design, ensuring uniform electrical characteristics across multiple units. This predictability contrasts sharply with wire-wound counterparts, where hand winding and manual assembly introduce variability [11].

1.1.4 Design Modularity and Integration

Another notable benefit of planar magnetics is the ease of modular integration. Because the winding structures are embedded within PCBs, additional components such as

semiconductors, capacitors, and sensors can be mounted directly on the same board. This co-location of passive and active components streamlines the power stage layout, reduces interconnection losses, and simplifies thermal management.

Multilayer PCB technology further enhances this integration by allowing arbitrary interconnection between different layers. This enables sophisticated winding arrangements such as interleaving, which significantly reduces leakage inductance and high-frequency losses [12].

1.1.5 Parasitic Control and Predictability

In traditional wire-wound magnetics, the parasitic parameters—such as stray capacitance and leakage inductance vary considerably across different production batches due to inconsistency in winding geometry and placement. In contrast, planar magnetic devices manufactured via PCB processes offer superior control over these parameters. Since the winding patterns are defined through computer-aided design and executed using precision etching and lamination, the parasitics remain consistent and highly predictable.

This predictability improves the design reliability of converters, filters, and inductors used in switched-mode power supplies and other high-frequency circuits. It also facilitates more accurate modeling and simulation during the design phase, which reduces the need for iterative prototyping and tuning [13, 14].

1.2 Design of Planar Transformers

Designing planar transformers involves multiple critical considerations including core material selection, winding configurations, and layout strategies to maximize efficiency and minimize losses.

1.2.1 Core Material Selection

Selecting appropriate core materials is essential for optimal transformer performance. Materials such as Ferrite, Nanocrystalline, and Amorphous alloys are preferred due to their excellent high-frequency magnetic properties, including high permeability, low core losses, and stable performance at elevated frequencies [15].

1.2.2 Winding Configurations and Interleaving

Optimal winding configurations in planar transformers frequently involve interleaved primary and secondary windings. Interleaving reduces leakage inductance by enhancing magnetic coupling, improving overall efficiency and performance. Additionally, careful design of winding layout and PCB trace geometry minimizes AC winding losses due to skin and proximity effects [16].

1.2.3 Thermal Management Strategies

Thermal management is crucial in planar designs due to their high-power density nature. Techniques such as spreading copper areas, thermal vias, and heat sinks integrated into PCB layers effectively manage heat dissipation. Advanced thermal simulation tools aid designers in predicting thermal performance and optimizing cooling strategies.

1.3 Winding Losses in Planar Magnetics

Winding losses in planar magnetic components primarily arise from high-frequency phenomena such as the skin effect, the proximity effect, and eddy current formation. These losses contribute significantly to the degradation of efficiency in high-frequency power conversion applications. Due to the distributed nature of current and magnetic field

interactions within planar structures, these effects are often more complex than in traditional wire-wound devices.

1.3.1 Skin and Proximity Effects

The skin effect is a frequency-dependent phenomenon where alternating current tends to concentrate near the surface of a conductor. As the operating frequency increases, the effective current-carrying depth of the conductor (known as the skin depth) decreases. This behavior leads to an increase in the alternating current (AC) resistance relative to the direct current (DC) resistance, thereby elevating the conduction losses in the windings.

In addition to the skin effect, proximity losses arise due to the interaction of magnetic fields between adjacent conductors carrying time-varying currents. These induced fields cause non-uniform current distributions that result in additional localized heating and further AC resistance. Planar windings, often fabricated as copper traces on multilayer printed circuit boards, are particularly susceptible to these effects because of their close spacing and geometric consistency.

To mitigate the impact of skin and proximity effects, planar magnetic designers employ several techniques. Increasing the conductor width and reducing the trace thickness can improve current distribution. Moreover, implementing interleaved winding structures across multiple PCB layers allows for magnetic field cancellation and reduced mutual coupling between conductors. These structural strategies, when supported by electromagnetic simulation tools, enable effective optimization of winding layouts for high-frequency operation [17].

1.3.2 Eddy Current Losses

Eddy currents are circulating currents induced within conductive materials due to time-varying magnetic flux. In planar magnetics, these losses can manifest in both the winding conductors and the magnetic cores. The magnitude of eddy current loss is

directly influenced by the thickness and conductivity of the material, as well as the rate of change of magnetic flux density.

To reduce eddy current losses in planar windings, the use of thin copper layers is favored. This constrains the formation of large circulating paths and limits energy dissipation. Additionally, using laminated core materials or materials with high electrical resistivity helps suppress eddy currents in the magnetic structure.

The overall design of planar magnetics must therefore account for the interaction between magnetic field distribution, current paths, and material properties. Advanced field-solving tools are frequently employed to analyze eddy current densities and inform design decisions. When properly addressed, eddy current mitigation techniques contribute significantly to the enhancement of efficiency and thermal performance in planar magnetic systems [18].

1.4 Leakage Inductance in Planar Transformers

Leakage inductance in planar transformers arises due to the incomplete magnetic flux linkage between the primary and secondary windings. Unlike ideal transformers, practical magnetic devices exhibit partial magnetic decoupling, where a portion of the magnetic field generated by one winding does not completely pass through the opposing winding. This effect contributes to energy storage outside the intended magnetic path, resulting in reduced coupling and potential voltage overshoots during switching transitions.

In high-frequency power electronic applications, leakage inductance is a critical design concern. Excessive leakage can lead to degraded efficiency, increased electromagnetic interference, and voltage spikes that stress semiconductor components. Moreover, in resonant and soft-switching converters, precise control over leakage inductance is necessary to shape the resonant tank behavior and ensure zero-voltage or zero-current switching [19].

1.4.1 Mitigation Techniques

Several design techniques are employed to minimize leakage inductance in planar magnetic structures. One of the most effective approaches involves interleaving the primary and secondary windings across multiple layers of the printed circuit board. This configuration allows the magnetic fields of adjacent layers to more effectively cancel or combine, thereby improving mutual coupling and reducing stray magnetic paths.

In addition to interleaving, optimizing the physical layout of the PCB traces is essential. Parameters such as trace width, spacing, and layer alignment directly influence the coupling coefficient. By minimizing the physical separation between current-carrying layers and maintaining symmetrical geometry, designers can reduce the uncoupled flux and improve the magnetic linkage.

The use of magnetic shielding is another strategy, particularly in designs that involve complex winding geometries or external field interference. Shielding layers help guide the magnetic flux through the intended paths and suppress stray field propagation, which can otherwise contribute to leakage effects.

Advanced electromagnetic modeling and simulation techniques are widely utilized in the design phase. Finite Element Analysis (FEA) tools, for example, allow for accurate prediction of magnetic field distribution and identification of leakage pathways. By iteratively refining the core geometry, winding configuration, and layer stack-up, designers can achieve optimized coupling performance tailored to specific frequency and load conditions.

Through these mitigation strategies, the impact of leakage inductance can be significantly reduced, leading to improved efficiency, enhanced control stability, and reliable operation of planar transformer-based systems [20, 21].

1.5 Winding Capacitance in Planar Transformers

Parasitic capacitance occurs between winding layers, significantly impacting high-frequency performance. Excessive winding capacitance can cause resonant behaviors, energy losses, and reduced efficiency [18].

1.5.1 Capacitance Reduction Techniques

Minimizing parasitic interwinding capacitance is a critical design requirement in planar magnetics, particularly for high-frequency power conversion applications. High levels of capacitance can reduce circuit efficiency, increase electromagnetic interference, and degrade signal quality.

One method to reduce interlayer capacitance is to increase the spacing between winding layers. This decreases capacitive coupling, although it must be balanced against the requirement for compactness and low leakage inductance. An alternative approach involves the use of insulating materials with low dielectric constants, which directly lowers the capacitance value.

Additional techniques include inserting grounded shields between winding layers to reduce common-mode noise and parasitic coupling. Split windings and selected interleaving patterns can also be used to control the trade-off between capacitance and inductance. Accurate modeling using simulation tools helps predict the performance impact of parasitics and enables optimization of the final design [22].

1.5.2 Planar Sandwiched Magnetics

Planar sandwiched magnetics are an advanced implementation of multilayer magnetic components, where alternating layers of magnetic cores and planar windings are arranged in a stacked configuration. This structure provides both compact geometry and improved thermal and electrical characteristics.

The sandwich construction enhances magnetic coupling and reduces leakage inductance by aligning core halves symmetrically around the winding layers. This symmetry also contributes to improved magnetic balance and reduced core loss. From a thermal perspective, the increased surface area and reduced thermal path support better heat dissipation, which is critical in high-density power systems.

Sandwiched configurations are particularly advantageous in medium-to-high power applications such as resonant converters and isolated DC-DC converters. These designs also enable better integration with printed circuit board technologies, allowing seamless connection to passive and active elements in the power stage.

Selection of suitable core materials such as ferrites or nanocrystalline alloys ensures stability across the required frequency range. Proper mechanical alignment and electrical balancing between layers are essential for consistent performance and manufacturability [23].

1.6 Applications of Planar Magnetics

Planar magnetic technology finds extensive applications across diverse sectors:

- Telecommunications and Data Centers: High-efficiency DC-DC converters.
- Automotive Electronics: Power conversion modules in electric vehicles.
- Aerospace: Compact, reliable power supplies for avionics.
- Medical Equipment: Miniaturized isolated power supplies.

Planar magnetics have substantially advanced power electronics, offering efficient, compact, and highly manufacturable solutions. Continuous research and innovation promise to address current design challenges, enhance efficiency, and extend application potential, firmly establishing planar magnetics as a foundational technology in modern power conversion systems [24, 25].

1.7 Problem Statement

This thesis addresses five key problem statements relevant to the advancement of electric vehicle (EV) systems and high-efficiency power electronics. Three of these problems are solved through the application of planar magnetic technology, while the remaining two are presented in the annexures focusing on the design of a biomedical power supply and the modeling of an advanced gate driver for traction inverter applications.

The first problem pertains to the conventional architecture of electric vehicles, which typically includes a dedicated Auxiliary Power Module (APM) for charging the auxiliary battery. The inclusion of this separate module increases system complexity and packaging volume. This thesis proposes a planar magnetics-based onboard charger design that integrates an auxiliary supply through a tertiary winding, thereby eliminating the need for an APM and offering a more compact and efficient solution.

The second challenge arises from the lack of a standardized conductive charging interface across different countries and vehicle manufacturers. Variations in connector types hinder universal compatibility and scalability. To address this, the thesis introduces a planar magnetics-based non conductive charging gun capable of delivering power to any EV. This approach aims to unify EV charging interfaces and improve user safety and convenience.

The third problem involves vehicle to vehicle (V2V) charging. In situations where access to charging stations is limited, a planar magnetics based V2V connector can enable one vehicle to supply power to another. The proposed solution leverages planar magnetics to create a compact and efficient V2V charging interface suitable for high frequency power transfer.

The remaining two problems are explored in the annexures. Annexure A presents the design and development of a USB Power Delivery (USB PD) enabled power supply tailored for biomedical applications such as ECG monitoring. Annexure B focuses on the

modeling of a gate driver for traction inverter systems, addressing challenges in high speed switching and protection features.

Together, these five problem statements form the foundation for the research contributions made in this thesis.

1.8 Methodology

The methodology adopted in this thesis is based on the simulation and performance evaluation of high frequency planar magnetics based systems targeted at advanced electric vehicle (EV) applications. The work addresses three core challenges: the elimination of a standalone Auxiliary Power Module (APM) in onboard EV chargers, the development of a universal non-conductive charging interface, and the simulation of a planar magnetics-based vehicle-to-vehicle (V2V) energy transfer mechanism. All simulations were conducted using MATLAB and Simulink environments to analyze circuit behavior, control strategies, and magnetic performance.

To address the first problem, a Dual Active Bridge (DAB) converter architecture is simulated, wherein a high-frequency transformer with a tertiary winding is used to supply auxiliary power. This configuration aims to eliminate the need for a separate APM by utilizing the same transformer core to derive auxiliary voltage. The simulation setup incorporates phase-shift control to ensure soft-switching, and the performance is analyzed with respect to flux balance, voltage regulation, and transformer utilization.

The second objective involves the simulation of a non conductive charging interface using inductive power transfer principles. Planar coil structures are configured as transmitter and receiver units within the simulation environment to evaluate magnetic coupling and power transfer. The aim is to develop a charging system that is independent of mechanical connectors and compatible across various EV platforms, thereby simplifying standardization and improving user safety.

For the third problem, a bidirectional V2V energy exchange system is simulated using DAB connected via planar magnetic elements. Control strategies based on dual phase-shift modulation are implemented to facilitate regulated energy transfer between vehicles in both directions.

The methodologies for two additional systems the USB Power Delivery-enabled power supply for biomedical applications, and the advanced gate driver for traction inverter applications—are discussed in Annexure A and Annexure B, respectively.

1.9 Outline of the Thesis

The structure of this thesis is organized as follows:

- **Chapter 2: Dual Active Bridge Control**

  This chapter presents the control strategies associated with the Dual Active Bridge (DAB) converter. It introduces the modulation techniques that are employed in the subsequent application-oriented chapters of this thesis.

- **Chapter 3: Planar Magnetics Based Onboard Electric Vehicle Charger with Auxiliary Supply**

  This chapter discusses the design and implementation of a planar magnetics-based onboard electric vehicle (EV) charger. The system eliminates the need for a dedicated auxiliary power module (APM), offering a more compact and integrated solution.

- **Chapter 4: Non Conductive Charging Gun for Electric Vehicle Charging**

  This chapter introduces a non conductive charging interface for EVs. The system utilizes planar magnetic structures to enable safe and efficient wireless charging, eliminating the need for physical contact during energy transfer.

- **Chapter 5: Planar Magnetics Based Vehicle to Vehicle (V2V) Connector**

  This chapter explores the development of a planar magnetics-based V2V connector

that facilitates direct energy transfer between electric vehicles. The system leverages compact magnetic integration to support peer-to-peer vehicle charging scenarios.

- **Chapter 6: Conclusion and Future Scope**

  This chapter summarizes the key outcomes of the research and outlines potential directions for future work in the areas of planar magnetics and power electronic integration.

- **Annexure A: Design and Development of Power Supply for Biomedical Applications**

  This annexure details the design of a power supply intended for ECG monitoring systems. The supply supports multiple modes of operation and communicates power delivery requirements via the USB Power Delivery (USB PD) protocol.

- **Annexure B: Modeling of an Advanced Gate Driver for Traction Inverter Applications**

  This annexure focuses on the modeling and simulation of a high performance gate driver tailored for traction inverter systems. The design emphasizes reliable switching, protection mechanisms, and compatibility with high-voltage traction architectures.

CHAPTER 2

Dual Active Bridge Control

2.1 Introduction

The Dual Active Bridge (DAB) converter is a high frequency isolated bidirectional DC DC converter that serves as the core component for High Frequency Link (HFL) Power Conversion Systems (PCSs). Its main advantage lies in its ability to achieve high power density, reduced weight, and minimized noise without compromising efficiency. DAB converters employ two full bridge circuits linked by a high frequency transformer, allowing efficient power transfer across isolated domains. This topology supports bidirectional power flow, making it suitable for applications such as energy storage systems, electric vehicles, and renewable energy integration.

The control strategy of DAB converters is critical to optimizing power transfer, ensuring stability, and minimizing power losses. Various methods have been developed to regulate the power flow within DAB converters, among which Single Phase Shift (SPS), Extended Phase Shift (EPS), Dual Phase Shift (DPS), and Triple Phase Shift (TPS) are the most prominent. Each strategy offers unique benefits in terms of efficiency, zero voltage switching (ZVS) range, and control complexity.

The following sections discuss these control strategies in detail, emphasizing their operational principles, advantages, and application scenarios.

2.1.1 Single Phase Shift (SPS) Control

Single Phase Shift (SPS) Control is the most widely used method for DAB converters due to its simplicity and effective power regulation. In SPS, the two full bridge circuits are controlled with a 50% duty cycle, with the power flow regulated by the phase shift between

the primary and secondary side. This phase shift determines the voltage difference across the transformer's leakage inductance, thereby controlling the magnitude and direction of power flow.

The key advantage of SPS is its ease of implementation and its ability to achieve Zero Voltage Switching (ZVS) under specific load conditions. However, it is limited by its high circulating current, which reduces efficiency, especially when the voltage amplitudes of the primary and secondary sides are mismatched [26–29].

2.1.2 Extended Phase Shift (EPS) Control

Extended Phase Shift (EPS) Control improves upon SPS by introducing an additional phase shift within one of the bridges. This modification allows for finer control of the power flow and enhances ZVS capabilities over a broader range of operating conditions. In EPS, the introduction of an inner phase shift reduces circulating power, minimizing current stress on the components and enhancing overall efficiency.

The primary benefit of EPS is its ability to extend the ZVS range, thus improving efficiency. It also provides better control during light load conditions, making it ideal for applications where power demands fluctuate significantly [30–33].

2.1.3 Dual Phase Shift (DPS) Control

Dual Phase Shift (DPS) Control further expands on EPS by applying phase shifts to both bridges. This dual modulation allows for even finer control of power flow, reducing circulating currents and optimizing efficiency. DPS is particularly effective in applications requiring bidirectional power flow, as it balances the energy transfer with minimal reactive power.

DPS's main advantage is its ability to achieve ZVS across a wider operating range while maintaining low current stress. This makes it a preferred choice for high power applications where efficiency and stability are critical [34, 35].

2.1.4 Triple Phase Shift (TPS) Control

Triple Phase Shift (TPS) Control introduces three degrees of freedom for power regulation, enhancing both control flexibility and efficiency. TPS enables independent control of the primary side phase shift, secondary side phase shift, and an additional phase adjustment between the two sides.

Although TPS provides the most granular control, it also introduces complexity in implementation and control design. Its application is best suited for scenarios demanding highly efficient bidirectional power flow with minimal losses [36–38].

2.2 Comparison of Control Strategies

The choice of control strategy for a DAB converter depends on application requirements such as power range, efficiency, and ZVS capability. SPS is optimal for simple applications with minimal control requirements, while EPS and DPS provide enhanced efficiency and ZVS over broader ranges. TPS offers the most control flexibility but at the cost of increased complexity.

A comparative analysis of these control strategies is presented in Table 2.1.

TABLE 2.1: Comparison of DAB Control Strategies

Control Strategy	**ZVS Range**	**Power Regulation**	**Circulating Current**	**Implementation Complexity**
SPS	Limited	Moderate	High	Low
EPS	Extended	Good	Moderate	Moderate
DPS	Wide	Excellent	Low	High
TPS	Very Wide	Superior	Very Low	Very High

2.3 Control of DAB and Communication Protocol

The architecture of the power electronics responsible for the power transmission in an electric vehicle (EV) is illustrated in Figure 2.1. The charging gun is designed to magnetically couple with the EV's body, maintaining an optimal air gap between the transmitting and receiving coils. This non contact method of power transfer leverages the efficiency of magnetic coupling to deliver energy without physical connectors.

Among various control strategies available for Dual Active Bridge (DAB) converters, Phase Shift Control (PSC) is one of the most widely adopted due to its simplicity and effectiveness in regulating power flow. In this technique, the active power reference, denoted as , serves as the primary control parameter. By adjusting , the direction and magnitude of power flow can be controlled. When is positive, the system operates in Grid to Vehicle (G2V) mode, supplying power from the grid to the EV. Conversely, a negative initiates Vehicle to Grid (V2G) operation, enabling bidirectional power flow back to the grid.

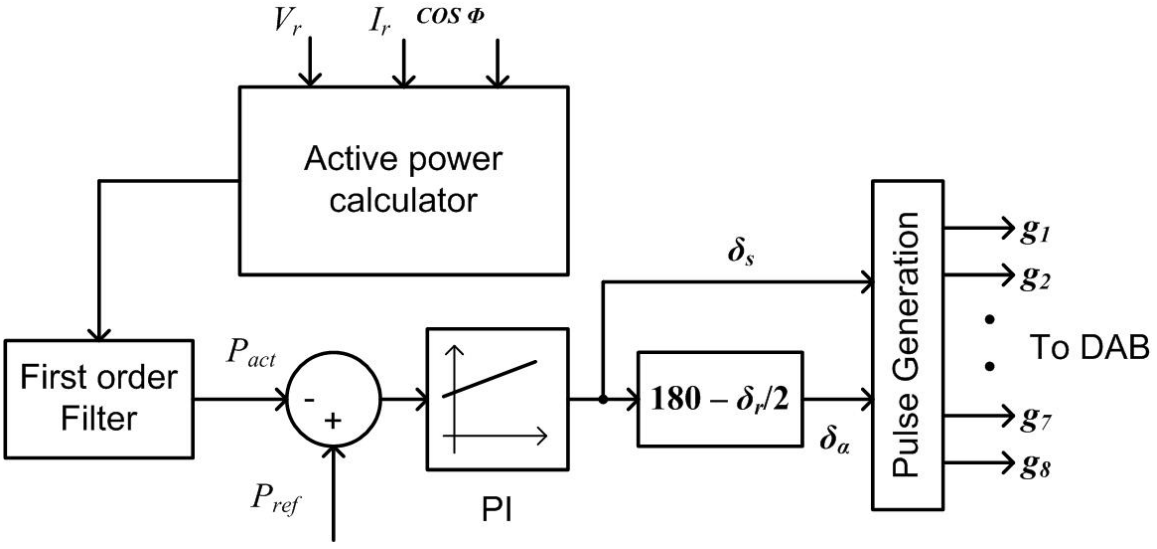


FIGURE 2.1: DAB Configuration in the Charging Gun

The value of is influenced by external factors such as battery health, state of charge (SOC), and other battery parameters. For analysis purposes, is considered constant. The phase shifts between the transmitting and receiving bridge legs are represented as and

respectively, while denotes the phase shift within the same side of the transmitting and receiving bridges. The total phase shift between the transmitting and receiving voltages, denoted by , is given by [39]:

$$\kappa = \delta_\gamma - \frac{\delta_\alpha}{2} + \frac{\delta_\beta}{2} \tag{2.1}$$

To simplify control, the phase shift between the transmitting side legs is maintained at a constant 180°. The value of can either be or , depending on whether the transmitting side voltage leads or lags the receiving side voltage. Assuming , the expression for simplifies to:

$$\delta_\gamma = 180^\circ - \frac{\delta_\beta}{2} \tag{2.2}$$

Equation 2.2 highlights that effective control of the secondary side phase shift allows for precise management of power flow in the DAB converter. The root mean square (RMS) values of the voltage and current at the receiving end are continuously monitored to generate an actual power value, , which is filtered through a first order filter for noise reduction. The filtered value is then compared with , and the error signal is processed through a Proportional Integral (PI) Controller to generate the required phase adjustments. This process ensures optimal pulse generation and power transfer.

Furthermore, a robust communication protocol is essential to facilitate real time power negotiation and status updates between the EV and the charging station. This link enables the dynamic adjustment of charging parameters, ensuring safe and efficient power transfer across different operating modes.

2.4 Conclusion

The DAB converter remains a cornerstone for high frequency bidirectional power conversion, with its control strategy being key to optimizing performance. Among the various control methods, DPS offers the best balance of efficiency, ZVS range, and manageable complexity for high power applications. Future improvements in control algorithms and power semiconductor technology are expected to further enhance the efficiency and application range of DAB converters.

CHAPTER 3

Planar Manganites Based Onboard Electric Vehicle Charger with Auxiliary Supply

3.1 Introduction

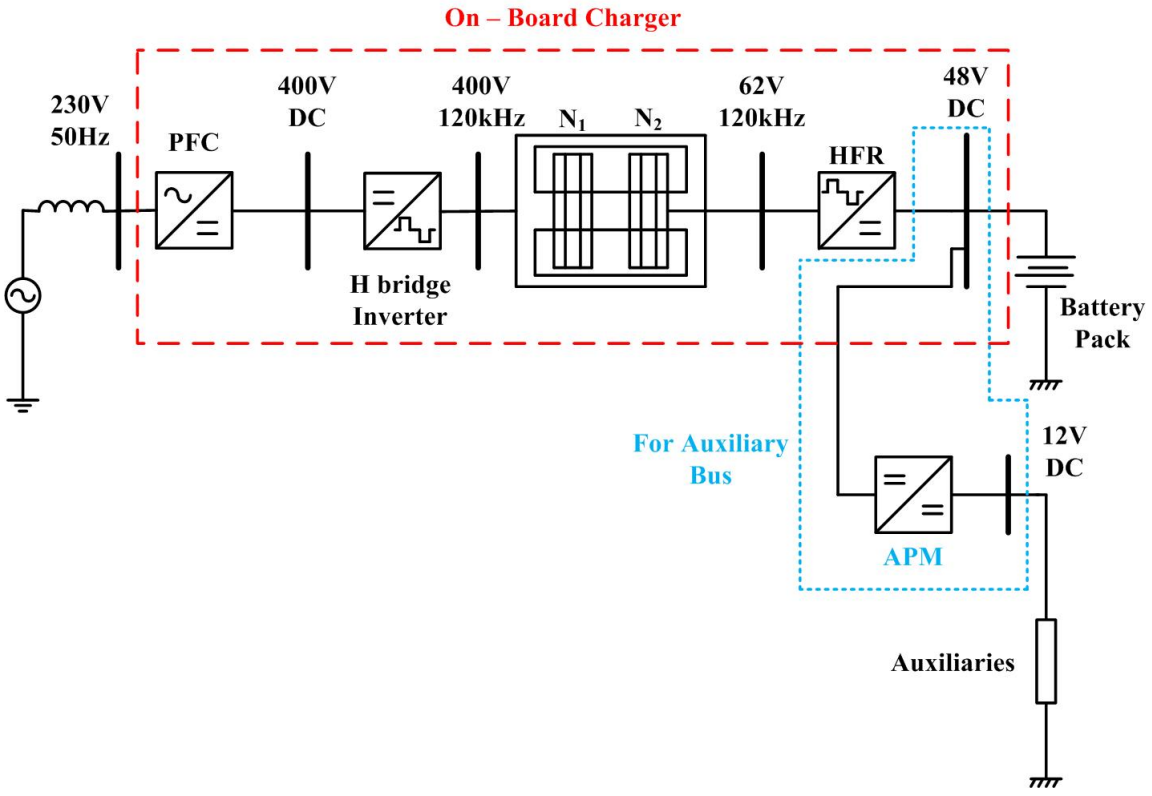


FIGURE 3.1: Conventional G2V Charger Topology

Figure 3.1 presents the conventional grid to vehicle (G2V) charging topology widely adopted in electric vehicle (EV) architectures. In this setup, the main battery pack (MBP), which supplies energy to the traction motor for vehicle propulsion, is recharged directly via the onboard charger (OBC). The OBC interfaces with the AC mains supply and performs AC DC conversion to charge the MBP efficiently. Concurrently, the auxiliary battery pack (ABP), which supports low voltage subsystems such as lighting, infotainment, dashboard instrumentation, and control electronics, is charged indirectly

from the MBP through an intermediate module known as the auxiliary power module (APM) [40]. The APM serves as a dedicated DC DC converter that steps down the high voltage DC output of the MBP to the lower voltage levels suitable for auxiliary loads [41, 42].

The APM is integral to maintaining a reliable and stable power supply for auxiliary systems across all operating states of the EV. In recent years, considerable research efforts have focused on enhancing the power density and reducing the overall cost and complexity of APM based systems. A substantial share of the cost associated with the APM arises from its physical packaging and thermal management infrastructure. While advances in mechanical design can offer limited gains, these are often insufficient to overcome the inherent challenges posed by volumetric constraints and heat dissipation, especially in configurations involving complex topologies [43–45]. Consequently, significant attention has been directed toward optimizing magnetic components, which constitute a core element in the power processing stage of such modules [46, 47].

To address these limitations, researchers have proposed several architectural innovations aimed at consolidating the APM and OBC functionalities. Building on this direction, the present work introduces a unified power conversion approach that eliminates the need for a separate APM. This is accomplished by embedding the auxiliary battery charging capability directly within the OBC through the use of planar magnetics. Specifically, a tertiary winding is incorporated into the planar transformer housed within the OBC. This tertiary winding enables direct power transfer to the ABP from the MBP, allowing the auxiliary battery to be charged not only during grid connected charging events but also while the vehicle is in motion.

The proposed strategy streamlines the EV powertrain by reducing the number of distinct modules, thereby minimizing system complexity and enhancing power density. In addition, this integration reduces the component footprint and supports miniaturization objectives, all while preserving the reliability and efficiency required for EV power management systems.

3.2 Proposed Design for Auxiliary Bus

In a typical grid to vehicle (G2V) configuration, as illustrated in Figure 3.2, the onboard charger (OBC) is interfaced directly with the utility AC grid to facilitate energy transfer to the vehicle's powertrain. The OBC architecture incorporates a power factor correction (PFC) stage, which serves the dual purpose of shaping the input current to follow the input voltage waveform and converting the AC input into a stable DC voltage, typically regulated at 400V. This regulated DC voltage serves as the input to the subsequent stage of the converter—namely, the dual active bridge (DAB).

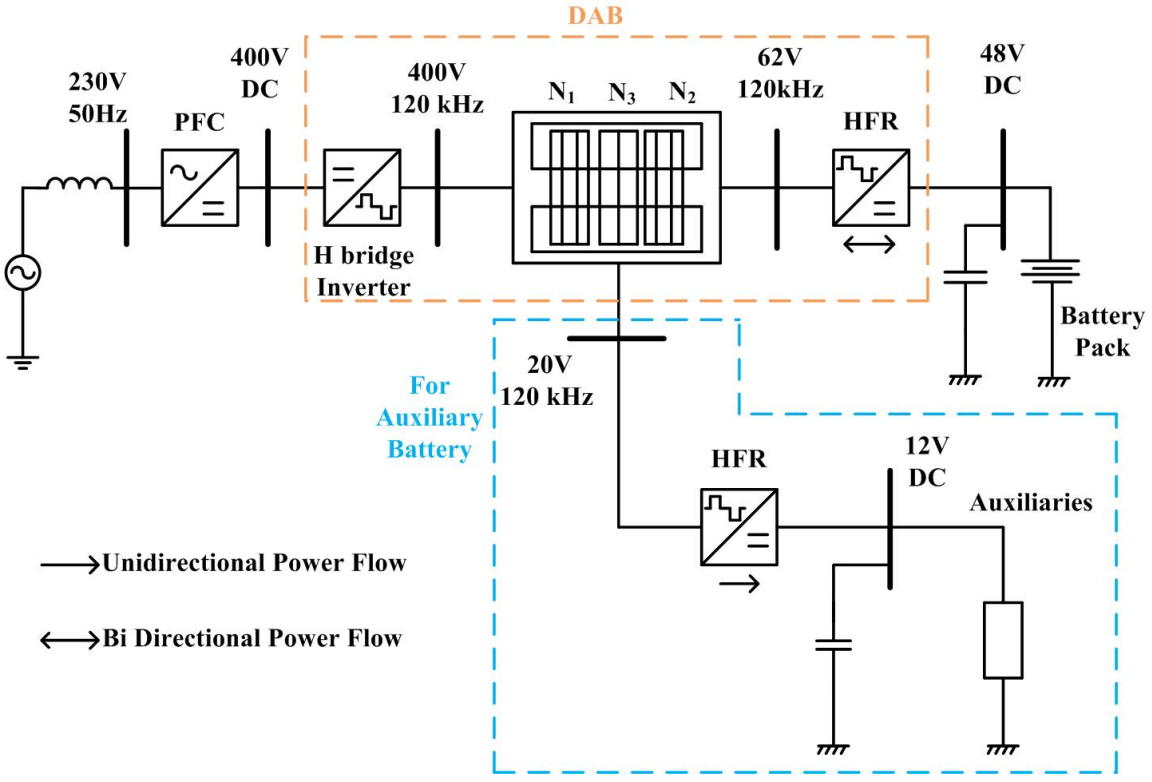


FIGURE 3.2: Schematics of Planar Magnetic Based Charger

The DAB topology comprises two H bridge converters interconnected by a high frequency transformer. On the primary side, an H bridge inverter generates a high frequency AC waveform, which is transmitted through the transformer and subsequently rectified by the high frequency rectifier (HFR) on the secondary side. This high frequency link, established via the transformer, enables the transfer of power to the main battery pack (MBP), which serves as the primary energy storage unit of the electric vehicle.

The operation of the OBC at elevated switching frequencies offers significant advantages. Higher switching speeds allow for a substantial reduction in the size of passive components—such as inductors and capacitors thereby contributing to overall system miniaturization and improved power density. Additionally, the incorporation of wide bandgap semiconductor devices, such as Silicon Carbide (SiC), further enhances the efficiency and thermal performance of the charger [48]. These devices are capable of withstanding higher voltages and operating at faster switching speeds with lower conduction and switching losses, making them highly suitable for modern high performance power electronic converters [49].

Traditionally, high frequency transformers used to create galvanic isolation in OBCs tend to be bulky and heavy, which adversely affects the power density and overall compactness of the charger. These limitations are particularly critical in EV applications where volume, weight, and thermal efficiency are key design constraints. To address these challenges, planar transformers have emerged as a promising alternative. Planar magnetic components offer several advantages over conventional wound core transformers, including a higher surface to volume ratio for improved thermal performance, superior heat dissipation, easier implementation of interleaved windings, and better manufacturing consistency due to their layered structure.

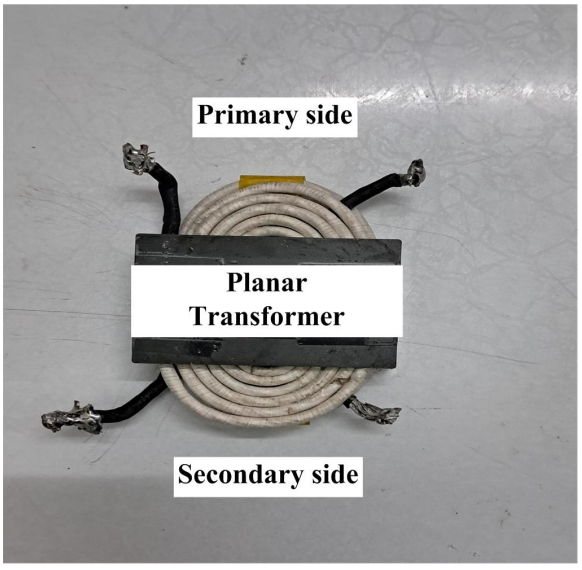


FIGURE 3.3: Planar Transformer

Figure 3.3 illustrates a two winding planar transformer used within the proposed OBC architecture. To further enhance system integration and reduce component count, a tertiary winding is introduced within the planar transformer. This additional winding facilitates the creation of an auxiliary DC bus, which provides a reduced voltage to a secondary HFR. The HFR, in turn, delivers regulated power to the ABP.

The integration of a tertiary winding into the planar magnetic structure enables the system to maintain a compact, low profile footprint while also supporting high frequency operation. This allows the OBC to deliver regulated power to both the main and ABP efficiently. The auxiliary bus can be energized either by the OBC during grid connected charging or directly by the main battery pack (MBP) when the vehicle is in motion. This ensures uninterrupted charging of the ABP across various operating scenarios. The bidirectional nature of power flow is managed through the dual active bridge (DAB), which continues to serve as the central element for controlling and routing energy within the system.

3.3 Modes of Operation for Auxiliary Bus

Figure 3.4 depicts the auxiliary bus that is designed by inserting the tertiary planar winding. For the analysis purpose a compensation network is considered and is represented by suffix fil or f. L_p, L_s, L_f and L_{aux}, represent the self inductance of the primary, secondary, compensation inductor, and tertiary coil for the auxiliary bus. The compensating capacitances are C_p, C_s, C_f, and C_{aux}. R_A is the representation of auxiliary loads. The compensation is provided in order to have constant voltage on both the sides. There are two modes that will be attainable. One is when both the battery packs will get charged by the OBC and thereby the need of APM is eliminated. Another is when EV is in motion, MBP will charge the ABP via auxiliary bus in which an HFR is introduced in order to get the 12V DC voltage.

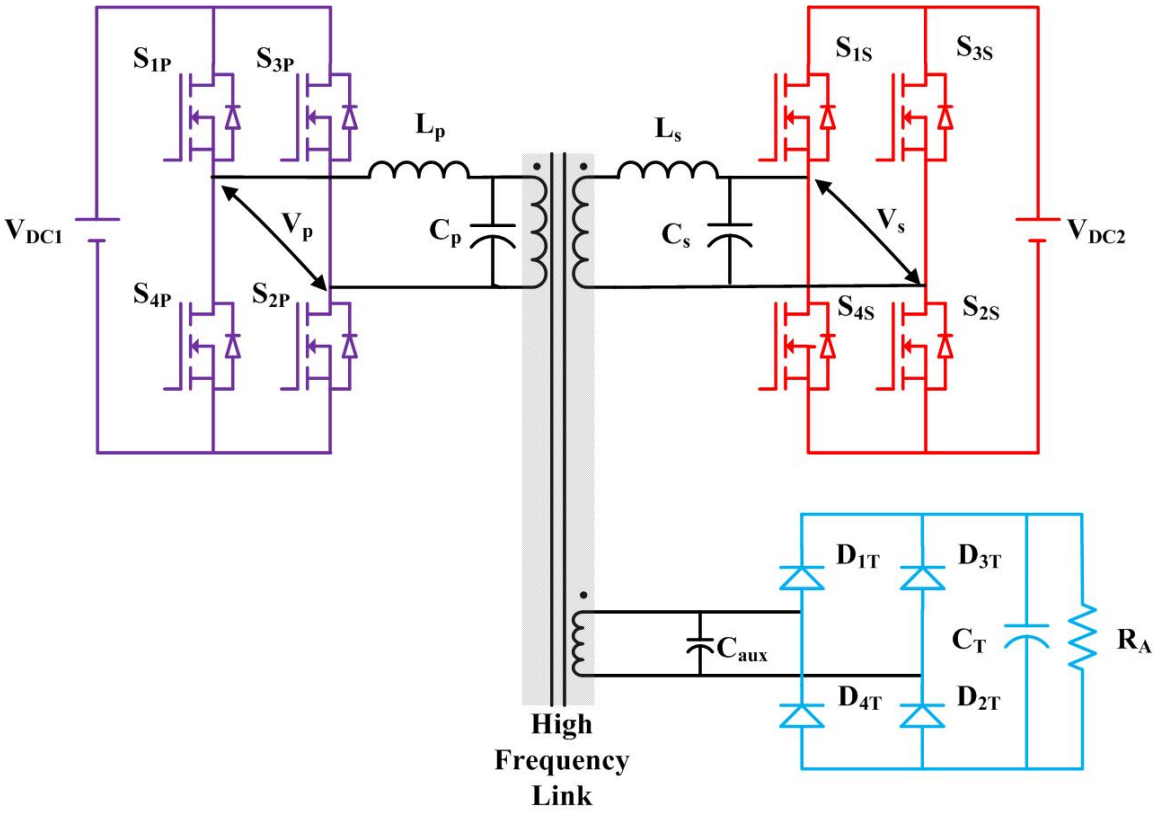


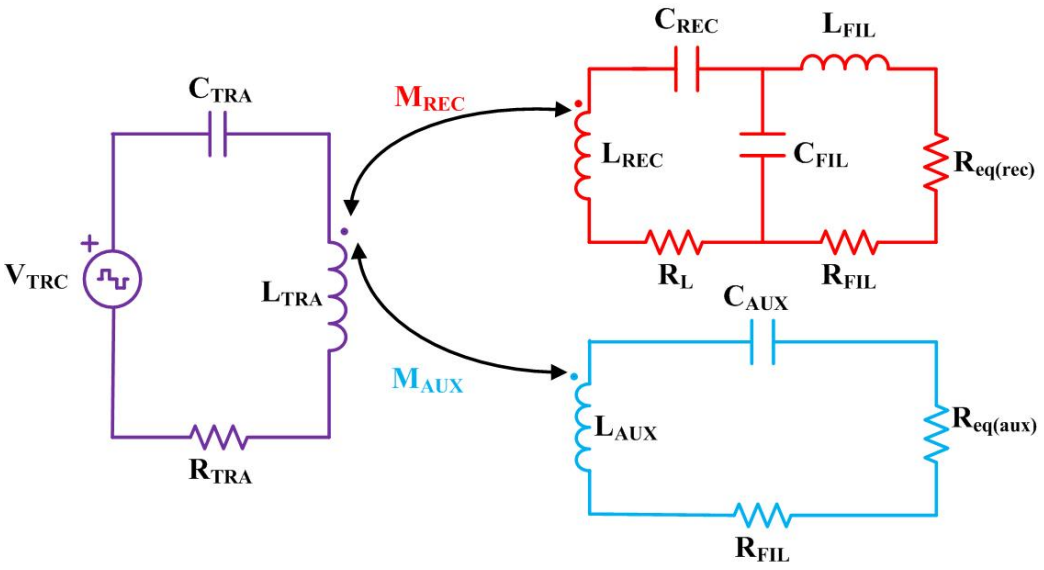
FIGURE 3.4: Schematics of Auxiliary Bus

3.3.1 Mode I: Both the MBP and ABP are Getting Charged By the OBC

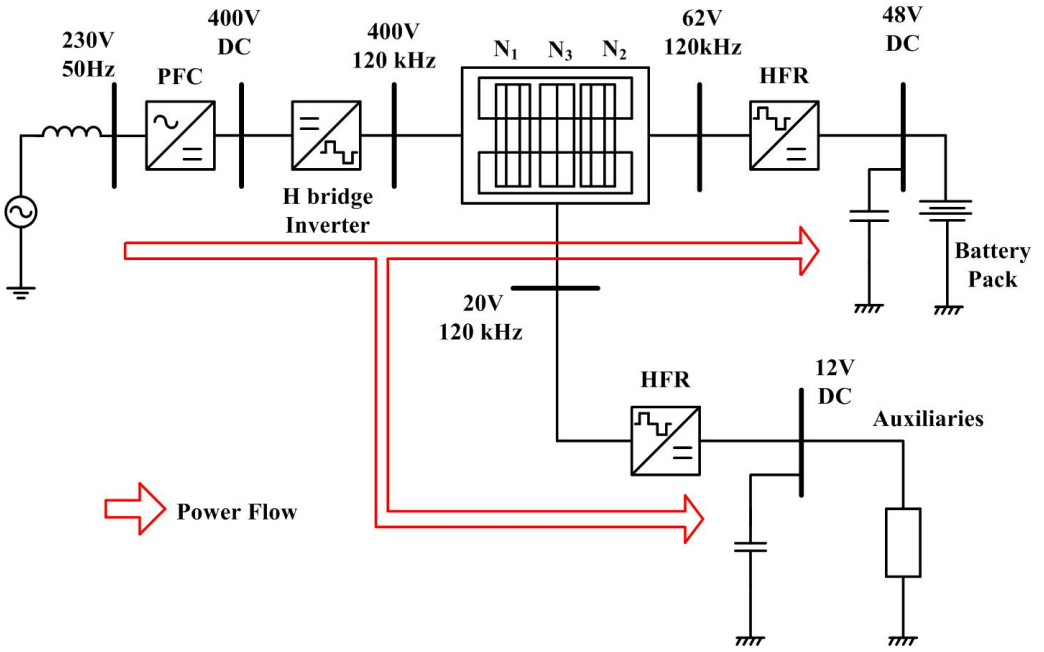
The proposed topology operates in Mode I, wherein both the MBP and the ABP are charged simultaneously through the OBC. Figure 3.5 illustrates the charging configuration corresponding to this mode of operation. Since power is being delivered from the primary side, it is referred to as the transmitting side, while the secondary and auxiliary branches, which receive power, are collectively referred to as the receiving side.

The system is characterized by several inductive components: L_{TRA}, L_{REC}, L_{AUX}, and L_{FIL}, which denote the equivalent inductances of the primary (transmitting) side, secondary (main battery) side, auxiliary bus, and the compensation network, respectively. Each of these inductive paths has an associated equivalent series resistance, designated as R_{TRA}, R_{REC}, R_{AUX}, and R_{FIL}.

Let V_{dc} represent the DC voltage applied on the primary side of the converter. The corresponding fundamental AC component of this DC voltage, inserted into the system



(A) Equivalent Diagram Representation of Mode I



(B) Power Flow in Mode I

FIGURE 3.5: Mode I Operation

through modulation, is denoted by V_{TRC}. The effective AC load resistances observed at the secondary and auxiliary sides are represented as $R_{eq(rec)}$ and $R_{eq(aux)}$, respectively. These parameters are evaluated using the Fundamental Harmonic Approximation (FHA), which enables simplified modeling of the power transfer characteristics in high frequency converters.

$$\begin{cases} V_{Tra} = \frac{2\sqrt{2}}{\pi} V_{dc} \\ R_{eq(rec)} = \frac{8}{\pi^2} R_{L(rec)} \\ R_{eq(aux)} = \frac{8}{\pi^2} R_{L(aux)} \end{cases} \tag{3.1}$$

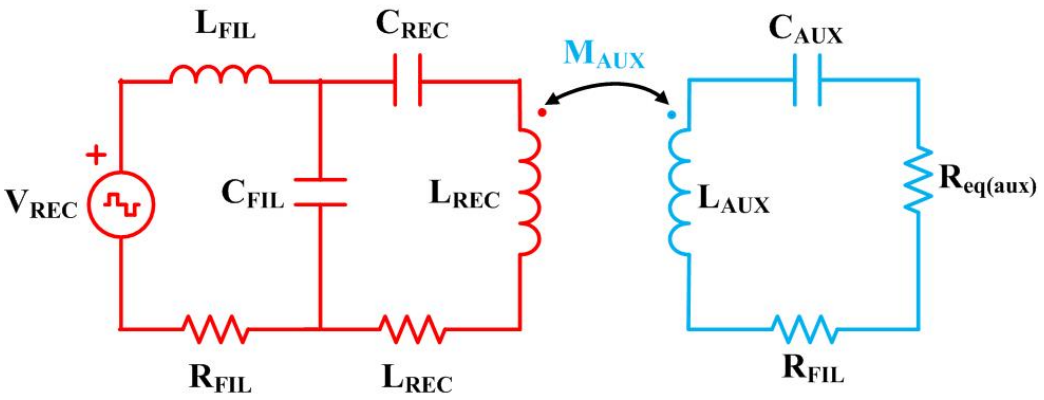
The output voltage and power can be defined as

$$\begin{gathered} V_{rec} = \frac{L_{rec}}{M} V_{dc} \qquad V_{aux} = \frac{M_{aux}}{M} V_{dc} \\ P_{\text{out }(rec)} = \frac{L_{rec}^2}{M_{rec}^2} \frac{V_{dc}^2}{R_{L(rec)}} \quad P_{\text{out (aux)}} = \frac{M_{aux}^2}{M_{rec}^2} \frac{V_{dc}^2}{R_{L(aux)}} \end{gathered} \tag{3.2}$$

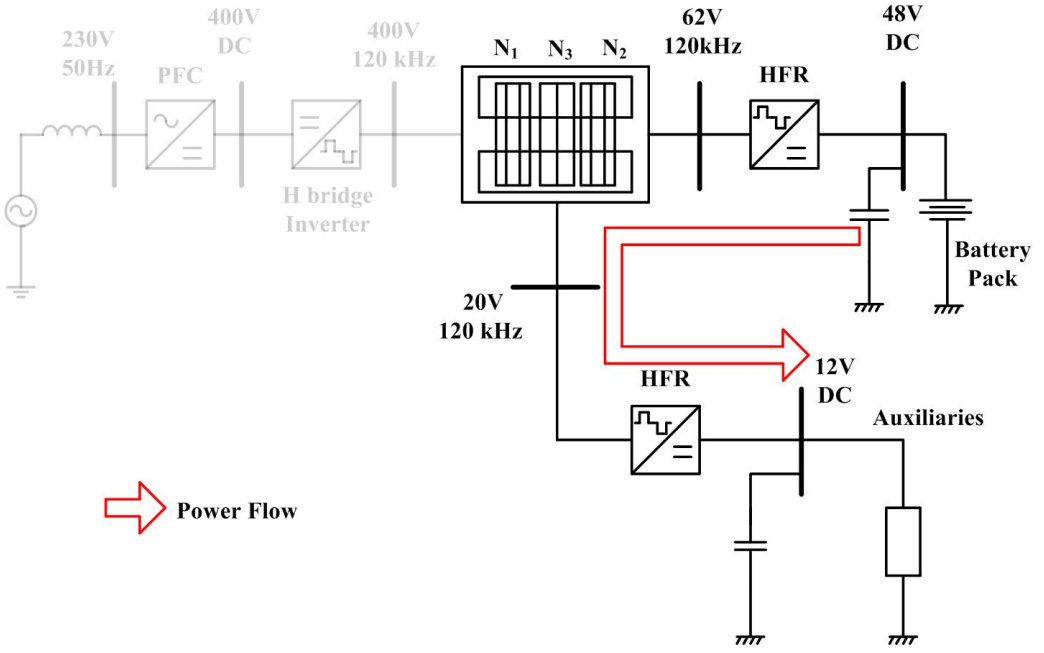
It can be seen from (3.2) that a constant voltage output for both the battery packs is obtained.

3.3.2 Mode II: MBP charges ABP During Running of EV

The proposed topology operates in mode II, in which the MBP supplies power to the motor for EV traction, simultaneously charging the ABP. The primary benefit of this mode is that the ABP will get charged even when EV is motion, ensuring that all auxiliaries receive an uninterrupted power supply.



(A) Equivalent Diagram Representation of Mode II



(B) Power Flow in Mode II

FIGURE 3.6: Mode II Operation

Figure 3.6 illustrates the charging process in mode II. Utilizing the fundamental harmonic approximation, the voltage of the MBP will be determined as following

$$V_{eq(rec)} = \frac{2\sqrt{2}}{\pi} V_{rec} \tag{3.3}$$

The result can be represented as

$$V_{aux} = \frac{M_{aux}}{L_{rec}^2} V_{\text{rec}} \qquad P_{out(aux)} = \frac{M_{aux}^2}{L_{rec}^2} \frac{V_{rec}^2}{R_{L(aux)}} \tag{3.4}$$

It can be seen from (3.4) that the MBP charges the ABP with a constant voltage.

3.4 Result and Discussion

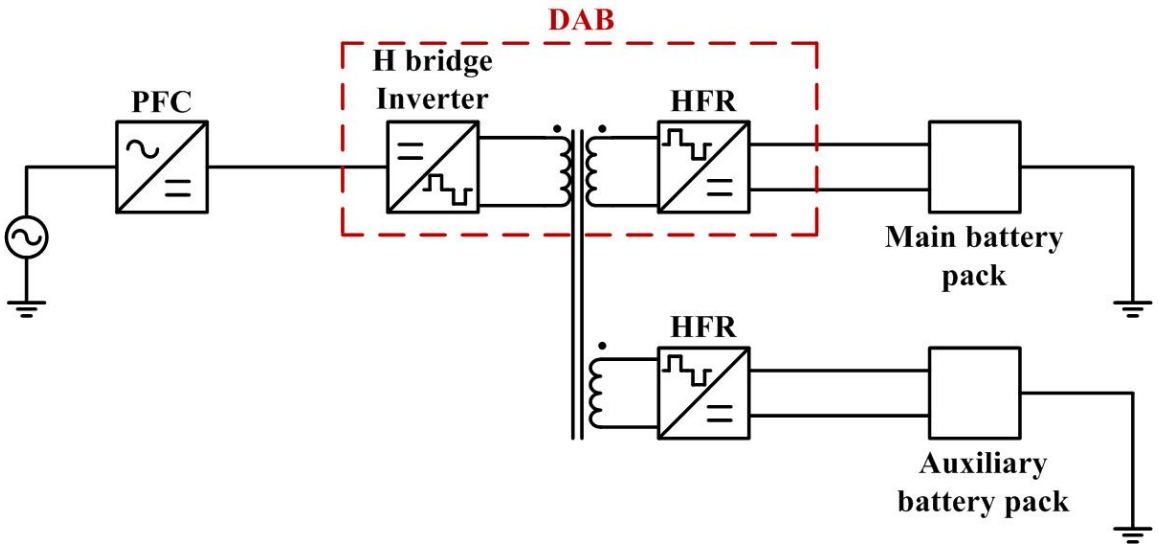


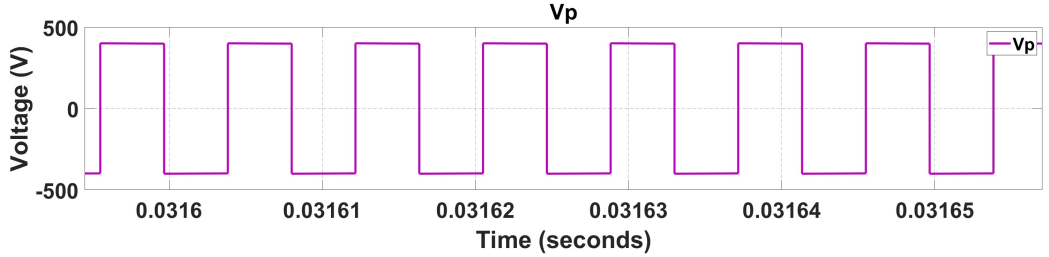
FIGURE 3.7: Schematics of Simulated System

The MATLAB based simulation was performed using the design parameters listed in Table 3.1. The circuit configuration, as illustrated in Figure 3.7, was implemented in MATLAB Simulink to evaluate the performance of the proposed system. The DAB converter is controlled using a phase shift modulation technique, which facilitates bidirectional power transfer between the MBP and the ABP. The control strategy of the DAB converter, as discussed in Chapter 2, is implemented.

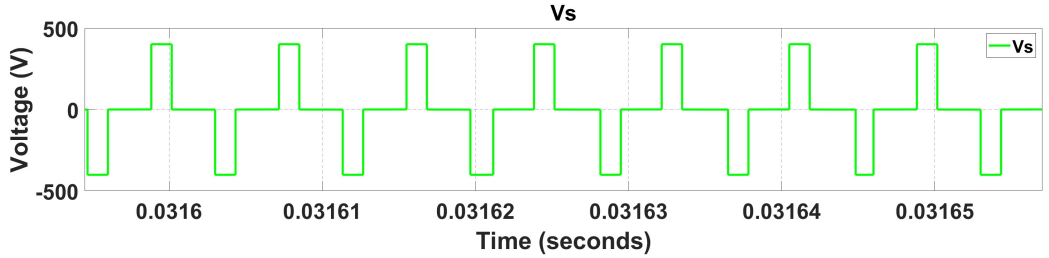
Key electrical quantities such as voltage and current at both the MBP and ABP terminals were observed and recorded during the simulation. The control of power flow through the DAB is primarily governed by the phase shift angle, which is regulated using a reference power signal, denoted as P_{ref}. This parameter plays a pivotal role in dictating the direction and magnitude of energy transfer. Specifically, the value of P_{ref} determines whether the DAB operates in a charging or discharging mode for the respective batteries. Therefore, accurate tuning of P_{ref} is essential for achieving the desired battery management functionality under various operating conditions.

TABLE 3.1: System Parameters

Battery Specifications (MBP)	**Parameter**
Battery Voltage	320V
Battery Charging Current	9A
Power	3.3kW
Battery Rating	90.4Ah
Battery Specifications (ABP)	**Parameter**
Battery Voltage	12V
Battery Charging Current	17A
Power	200W
Battery Rating	30Ah
DAB specifications	**Parameter**
Switching frequency	120kHz
Mutual Inductance	0.486μH
Coupling factor	0.96
Controller parameters	**Parameter**
secondary side k_p, K_i	0.025,25
Power reference	3300W
Transformer Configuration	**Parameter**
Number of turns N_1:N_2:N_A	20:20:1



(A) Primary voltage



(B) Secondary voltage

FIGURE 3.8: DAB Converter Primary and Secondary Side Voltages

Figure 3.8 presents the voltage waveforms observed on both the primary and secondary sides of the DAB converter. A distinct phase shift between the two voltage signals is clearly visible, indicating that the phase shift control strategy has been successfully implemented. This phase displacement is fundamental to the operation of the DAB, as it directly governs the direction and magnitude of power transfer between the MBP and the ABP. The observed waveforms confirm the correct functioning of the modulation scheme and validate the effectiveness of the control methodology adopted in the simulation.

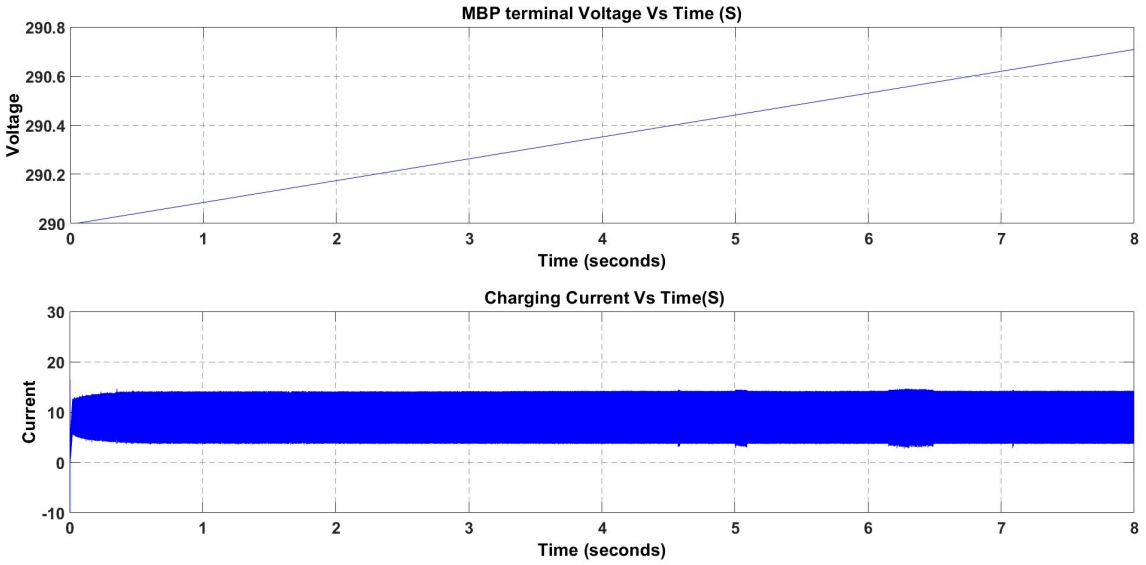


FIGURE 3.9: Charging Voltage and Current of MBP at Actual Ah

Figure 3.9 illustrates the voltage and current profiles of the MBP during the charging process, simulated using its actual ampere hour (Ah) rating. As shown in the figure, the charging current remains nearly constant throughout the process, while the voltage gradually increases a behavior that is consistent with standard constant current/constant voltage (CC/CV) charging protocols. This confirms that the implemented topology effectively meets the specified charging requirements of the MBP. The ability of the system to maintain a stable current while allowing the voltage to rise reflects proper control over the DAB power transfer and validates the suitability of the proposed configuration for battery management applications.

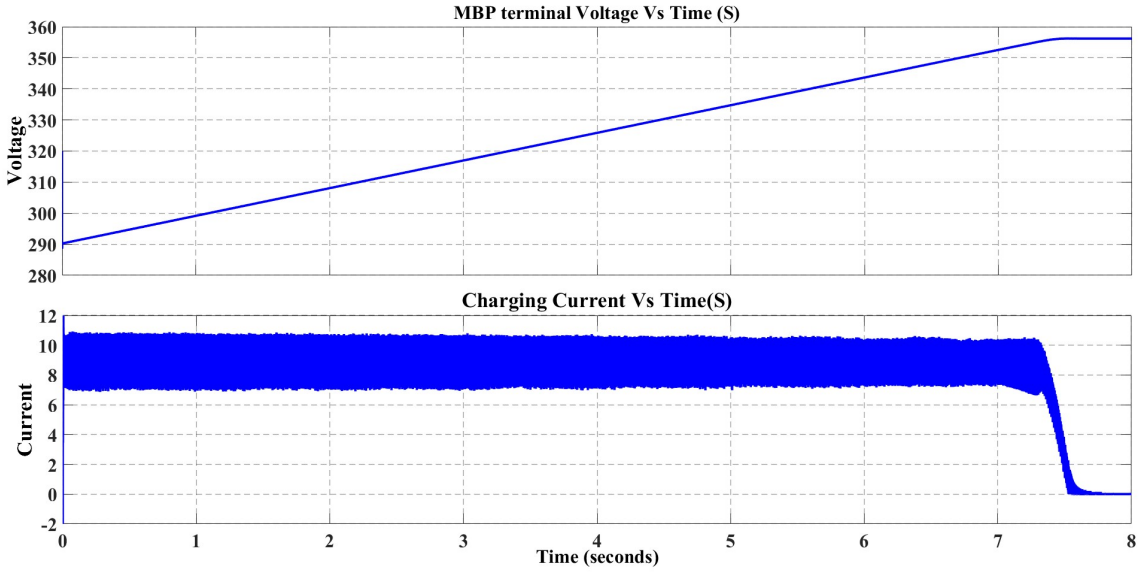


FIGURE 3.10: Charging Voltage and Current of MBP at Reduced Ah

Due to limitations inherent to the simulation tool, the ampere hour (Ah) rating of the battery was scaled down to facilitate a complete visualization of the charging cycle within a reasonable simulation time. Figure 3.10 depicts the full charging profile of the MBP under these conditions. The results demonstrate that the MBP is successfully charged via the OBC, validating the effectiveness of the proposed power transfer architecture.

Furthermore, the control strategy employed based on phase shift modulation proved capable of regulating the charging process within the desired voltage limits. The battery voltage was maintained within its specified threshold, thereby ensuring safe and efficient charging. This confirms that the implemented control technique is well suited for managing the voltage dynamics of the MBP during charging, even under adjusted simulation parameters.

Figure 3.11 illustrates the voltage and current waveforms observed at the terminals of the ABP during both modes of operation. The results confirm that a stable and consistent voltage and current are maintained at the auxiliary bus under both conditions when the ABP is charged via the OBC in Mode I, and when it is powered by the MBP during vehicle operation in Mode II. This stability is critical to ensuring the reliable and efficient charging of the ABP. The observed performance validates the proper functioning of the auxiliary bus architecture, as well as the control strategy implemented to regulate its

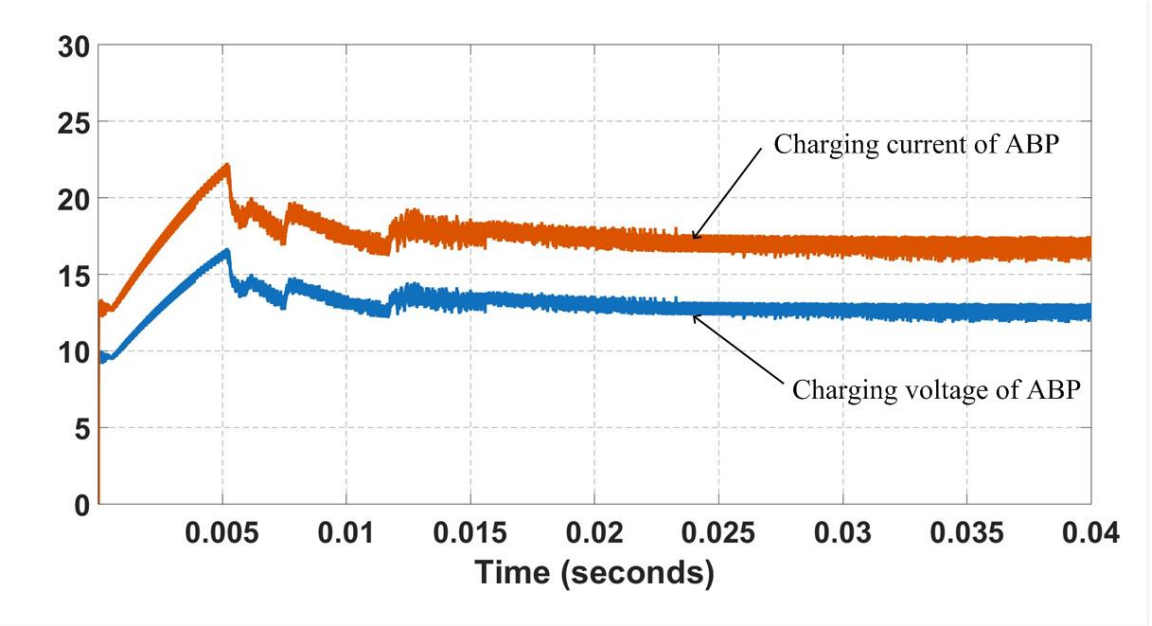


FIGURE 3.11: Charging Voltage and Current of ABP

output. The simulation thus confirms that the auxiliary charging mechanism operates within the required parameters.

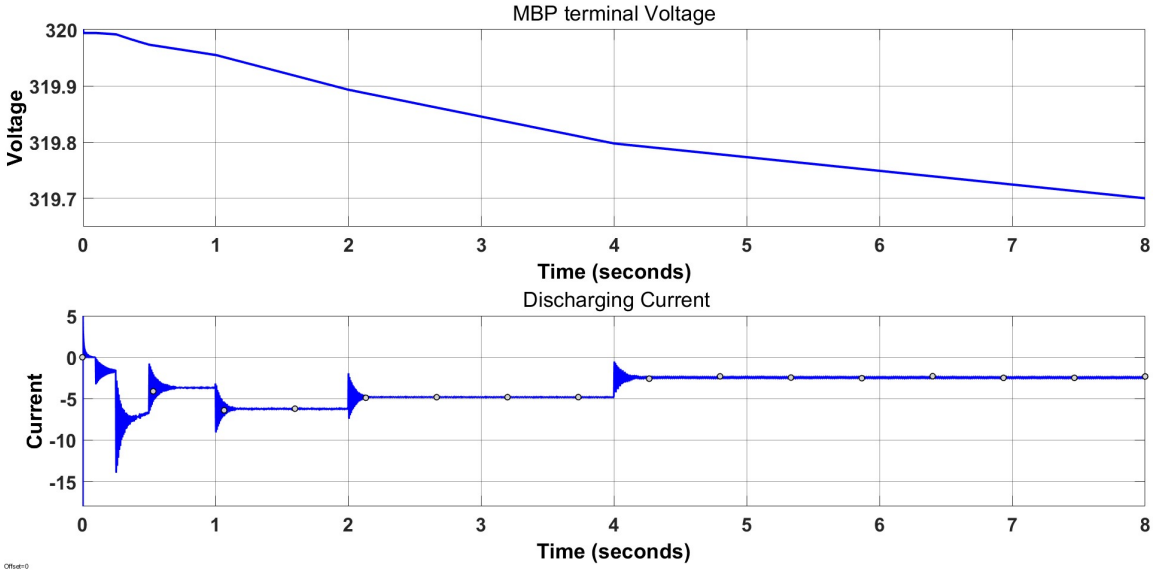


FIGURE 3.12: MBP Discharging in Mode II to Charge ABP

Figure 3.12 presents the discharging characteristics of the MBP and the corresponding charging profile of the ABP during Mode II, which represents the vehicle's running condition. During this mode, the MBP supplies power to the ABP. The initial current is limited, reflecting the controlled nature of the charging process. Since the ABP

is not completely discharged in this case, the current demand at the onset of charging is relatively lower. The simulation is performed using the actual ampere hour rating of the battery, thereby offering a realistic representation of the charging scenario. These results further affirm that the proposed topology supports the ABP's charging requirements without compromising the system's stability or performance.

3.5 Conclusion

This chapter presented an architecture for simultaneous charging of MBP and ABP using a shared high frequency link established through a planar transformer. A tertiary planar coil was introduced to form an auxiliary bus, enabling the OBC to charge both MBP and ABP, thereby eliminating the requirement for a separate APM. During vehicle operation, the MBP continues to power the ABP, ensuring stable auxiliary bus voltage and current. The charging parameters voltage and current for both MBP and ABP were successfully achieved and validated through MATLAB/Simulink simulations, confirming the feasibility and effectiveness of the proposed configuration.

CHAPTER 4

Non Conductive Gun for Electric Vehicle Charging

4.1 Introduction

Electric vehicles (EVs) are progressively replacing internal combustion engine (ICE) vehicles, driven by growing environmental concerns and the global emphasis on sustainable transportation. To support the transition toward EVs, several charging techniques have been developed and implemented worldwide. These charging approaches can broadly be categorized into two main types: (i) conductive charging and (ii) non conductive charging, also known as wireless power transfer (WPT). In conductive charging, power is transferred from the grid to the vehicle through a physical interface, typically using a charging connector or gun [50, 51].

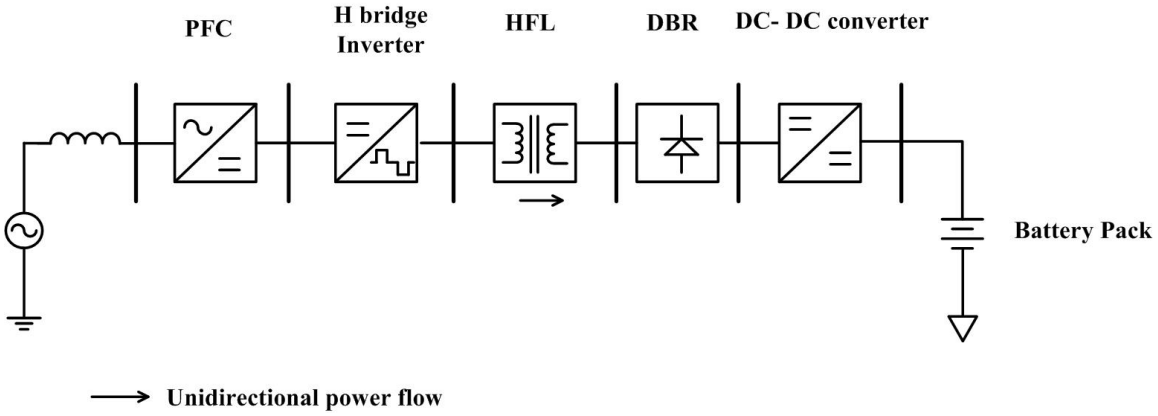


FIGURE 4.1: Schematic of Conductive Charging

Figure 4.1 illustrates a schematic of a conventional conductive charging setup, representing a grid to vehicle (G2V) power transfer scenario. While conductive charging is widely adopted, it presents several challenges. These include the need for manual user intervention during the connection and disconnection process, incompatibility between connectors used by different EV manufacturers, and increased complexity in managing

protocol standards as charging rates and voltage levels rise. These issues highlight the need for a universal and standardized charging interface [52, 53].

WPT has emerged as a potential alternative to address many of the limitations associated with conductive charging. WPT eliminates the need for direct physical contact, offering improved safety and convenience. However, WPT systems face challenges of their own, notably reduced coupling efficiency as the physical separation between the transmitting and receiving coils increases. To mitigate this, WPT systems typically operate at higher switching frequencies typically in the range of 85–90kHz to enhance magnetic coupling and support adequate power transfer [54].

To overcome the drawbacks of both conductive and WPT methods, this chapter proposes a novel charging gun that combines the advantages of both techniques. The proposed solution is based on planar magnetics, which are highly suitable for operation at elevated switching frequencies, such as those found in onboard chargers (OBCs). By leveraging a planar magnetic based coil, the charging gun eliminates the need for traditional connectors and their associated complexities. Since different EV platforms use varying types of connectors, this approach helps standardize the charging interface, reducing design variability and enhancing user convenience.

Overall, the proposed planar magnetic based charging gun provides a compact, efficient, and universal solution for EV charging, integrating the reliability of conductive systems with the flexibility and safety of wireless power transfer.

4.2 Drawback of Different Charging Typologies

Conductive charging remains the most widely adopted method for EV charging due to its inherent simplicity and relatively high efficiency. It offers a straightforward physical interface and direct energy transfer, making it a dependable solution in most applications. However, conductive charging requires a dedicated connector to establish the link between the EV and the grid. As various EV platforms utilize different connector types,

interoperability becomes a challenge. Among these, the CCS/Combo 2 connector, shown in Figure 4.2, is the most commonly used. This connector supports both AC slow charging and DC fast charging modes, providing versatility across multiple EV systems [55, 56].

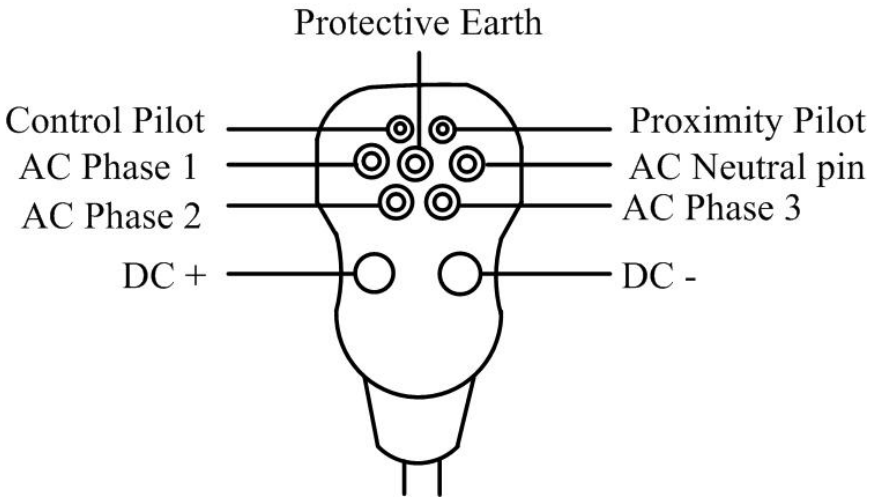


FIGURE 4.2: Schematic of CCS Combo 2

As charging levels increase, the physical structure of these connectors becomes more complex and bulkier. The mechanical integration of the charging assembly into the vehicle becomes cumbersome, particularly in high power configurations. Handling such large and heavy connectors becomes increasingly impractical, especially when dealing with medium and heavy duty EVs. These limitations highlight the need for an alternative approach, where WPT emerges as a potential solution to enhance user convenience and operational safety [57].

WPT systems utilize a pair of magnetically coupled pads—one for transmission and the other for reception. The spacing between these pads varies depending on vehicle ground clearance. WPT inherently provides galvanic isolation between the transmitting and receiving sides, mitigating the risk of electric shock and enhancing safety. This feature becomes particularly beneficial when charging large EVs. Despite its advantages, WPT has certain drawbacks. The system is highly sensitive to misalignment between the pads, which significantly impacts power transfer efficiency. Additionally, the control algorithms are relatively complex, and the system is susceptible to EMI. The inherently

low coupling coefficient due to the spatial separation between coils reduces overall system efficiency compared to conductive charging. To counteract this, compensation networks using passive components are introduced, which inadvertently reduce the power density of the OBC. However, with the appropriate DAB control, bidirectional power flow can be effectively managed within the system [58].

Both conductive and WPT methods exhibit unique challenges that limit their scalability and practicality in evolving EV infrastructure. These limitations have motivated the exploration of an alternative solution in the form of a novel charging gun architecture that employs planar magnetic coils for power transmission. The proposed design eliminates the dependency on bulky connectors and mitigates alignment and safety concerns associated with WPT. By combining the benefits of both technologies while addressing their respective shortcomings, the planar magnetic based charging gun presents a compact, efficient, and robust solution for modern EV charging applications.

4.3 Design of Non Conductive Charging Gun

Figure 4.3 illustrates the schematic of a non conductive EV charging arrangement based on the proposed charging gun architecture. In this configuration, the EV charging station incorporates a PFC stage to regulate the power factor close to unity. In addition to improving power quality, the PFC circuit boosts the traditional 230V AC supply to a regulated 400V DC output, which serves as the input for the next power conversion stage.

The elevated DC voltage is then supplied to a DAB, which consists of an H bridge inverter operating at high frequency. The DAB converts the 400V DC into high frequency AC, establishing a high frequency link through which energy is transferred. This link is formed using magnetically coupled planar coils, engineered for higher coupling coefficients. The planar magnetic structure inherently supports high frequency operation, resulting in greater energy transfer efficiency and higher power density.

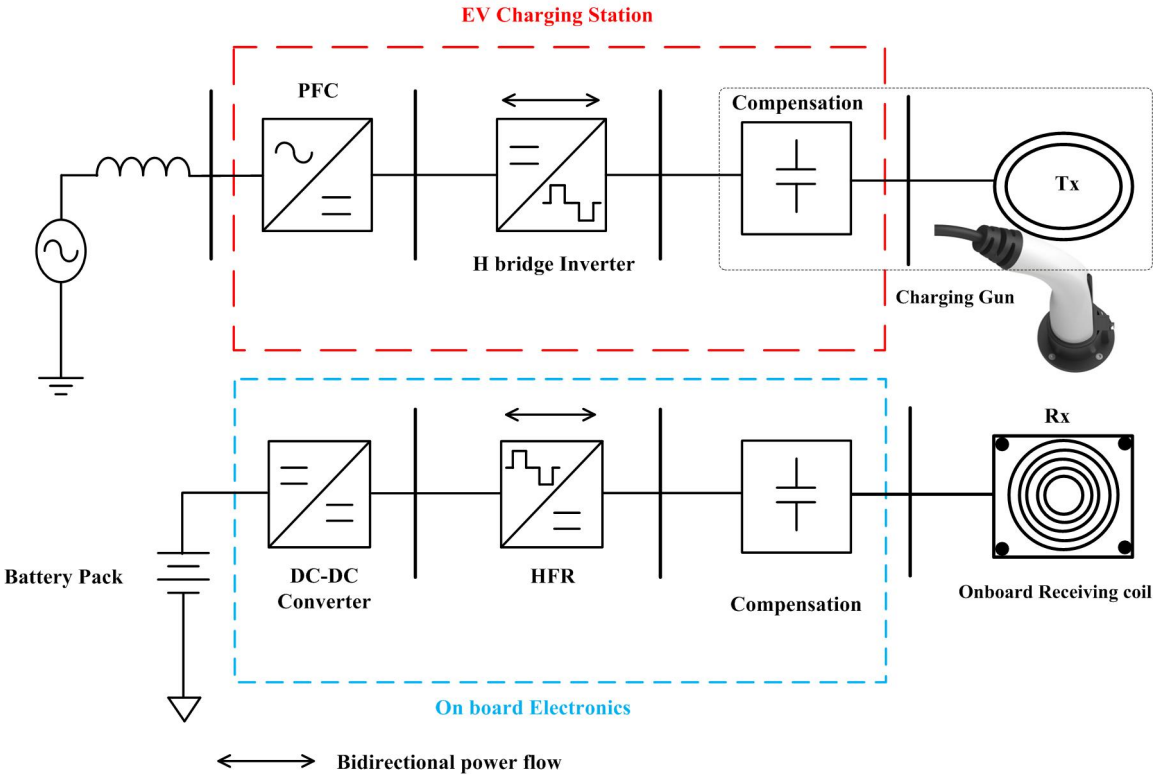


FIGURE 4.3: Schematic of Non Conductive EV Charging Arrangement

One of the key advantages of the proposed topology is the relatively minimal modification required compared to conventional conductive charging guns. On the receiver side, the high frequency AC is rectified using an HFR, followed by a DC DC converter that steps down the voltage to the appropriate battery level required for charging the EV.

The planar coils employed in the charging gun contribute to increased system energy density and improved compactness. A notable benefit of this system is its reduced sensitivity to misalignment, a common challenge in traditional WPT systems. Owing to the tight magnetic coupling of the planar coils, the spatial tolerance during charging is significantly improved, minimizing performance degradation due to alignment errors.

However, the system is not entirely free from losses. To enhance overall efficiency, a compensation network is integrated into the topology [59, 60]. The role of this network is to offset reactive components and mitigate energy losses, ensuring more efficient power

transfer. The specific configuration of the compensation network is chosen based on the level of efficiency enhancement required, and can be tailored accordingly.

In the context of WPT systems, the fundamental operating frequency—at which resonance and optimal power transfer occur—is governed by Equation (4.1):

$$\omega = \frac{1}{\sqrt{L_\alpha C_\alpha}} = \frac{1}{\sqrt{L_\beta C_\beta}} \tag{4.1}$$

Where L_α, C_α, L_β, C_β are the inductance and capacitance of compensating circuit used for transmitting, receiving side respectively. M is the mutual inductance between the coils. The coupling factor between these coils k, is given as (4.2),

$$k = \frac{1}{\sqrt{L_\alpha L_\beta}} \tag{4.2}$$

The total inductance L_T can be found out experimentally by connecting both the coils in series and is given by (4.3)

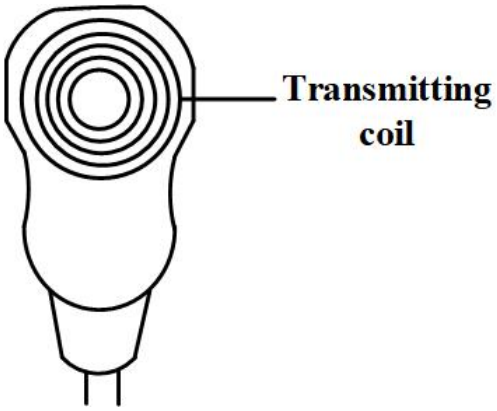
$$L_T = L_\alpha + L_\beta \mp 2M \tag{4.3}$$

The quality factor is measure by which the planar coil which is designed can be termed efficient. The quality factor is the main factor which contributes to maximum efficiency as,

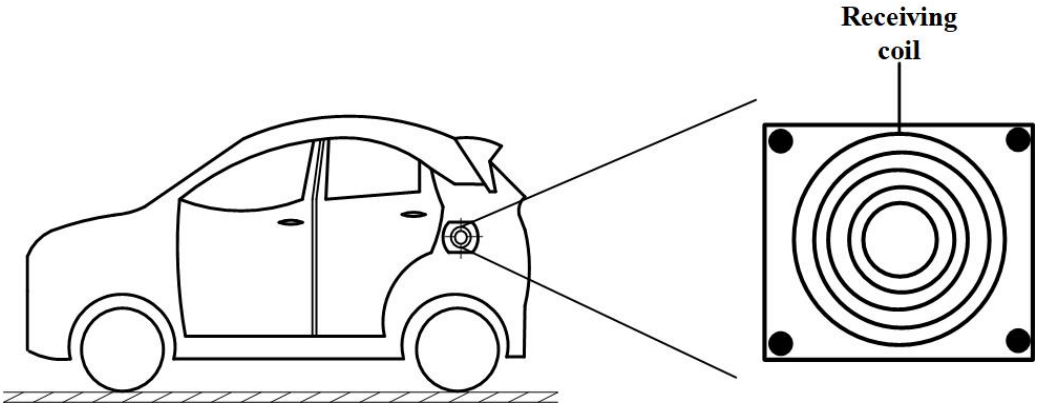
$$\eta_{\max} = \frac{k^2 Q_\alpha Q_\beta}{\left(1 + \sqrt{k^2 Q_\alpha Q_\beta}\right)^2} \tag{4.4}$$

In (4.4), Q_α, Q_β is the Q factor for transmitting and receiving side planar coils respectively. There are different shapes in which the planar coil can be designed.

Figure 4.4 illustrates the proposed arrangement that integrates both conductive charging and WPT functionalities into a unified system. In this configuration, the



(A) Transmitting Coil on Charging Gun



(B) Receiving Coil on Vehicle Body

FIGURE 4.4: Charging Gun Configuration

charging gun is equipped with a transmitting coil designed to deliver power wirelessly. This coil establishes a magnetic link with the receiving coil embedded in the EV's body structure. The receiving coil captures the transmitted power and delivers it to the onboard power electronics, which condition the energy and facilitate battery charging.

At the commencement of the charging process, the transmitting and receiving coils become magnetically coupled. This coupling is maintained throughout the duration of power transfer, ensuring stable and efficient energy delivery. For the system to operate reliably, communication between the EV and the charging station is essential. This communication protocol is responsible for initiating the charging sequence, negotiating power levels, and maintaining safety parameters during the operation.

The DAB plays a crucial role in enabling controlled bidirectional power flow between the charging station and the vehicle. By regulating the phase shift within the DAB, precise

control over the amount and direction of energy transfer is achieved. This ensures that the power delivered to the EV is both efficient and compliant with the required charging specifications.

4.4 Communication When Charging

The WPT functionality embedded in the proposed topology can be effectively managed through various control strategies, including charging station side control, EV side control, or a dual side control approach. Among these, dual control and charging station side control are generally preferred in practical implementations. This is primarily because the EV side controller may not always be available or active during the initial stages of charging. Additionally, implementing EV side control often necessitates additional circuitry, which increases complexity and cost.

Charging station side control also provides an added layer of safety. In the event of faults such as a short circuit, grid side intervention becomes essential to mitigate risks and protect system components. Therefore, employing either dual control or charging station side control enhances the safety, reliability, and adaptability of the overall WPT system in EV applications.

To ensure seamless power transfer and coordination between the EV and the charging station, various communication standards and protocols have been developed by recognized international bodies such as ISO and SAE. For WPT systems, the ISO 15118-8 standard defines the communication framework necessary to establish and maintain power transfer between the EV and the charging station. This standard serves as an extension of ISO 15118-3, which governs the communication architecture for wired charging systems [61].

The proposed topology employs communication based on the SAE J2847 family of standards, specifically adhering to the SAE J2847-6 protocol. This protocol defines a series

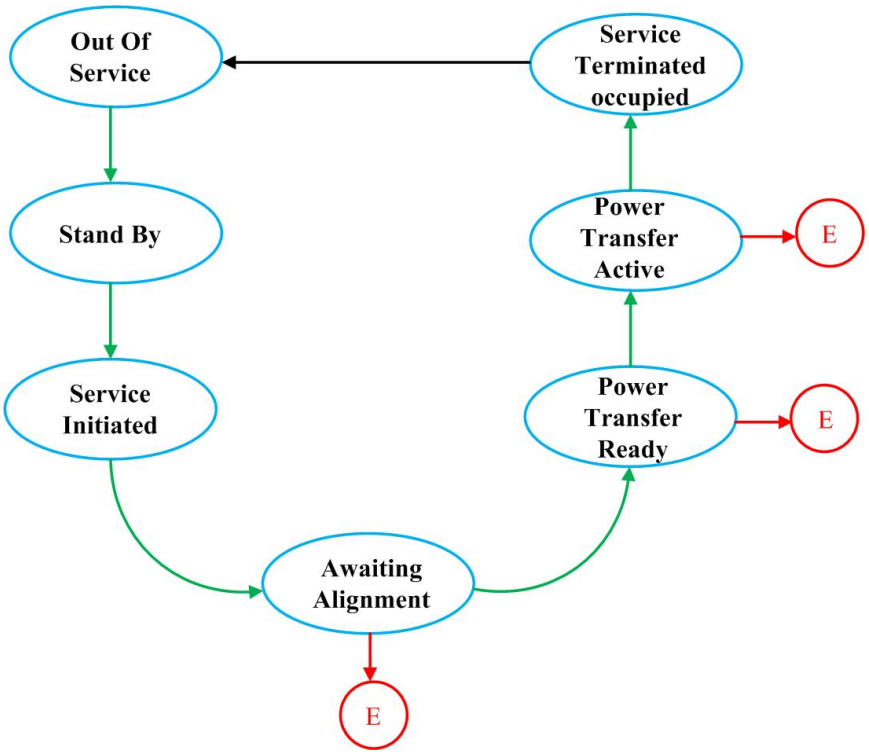


FIGURE 4.5: State Diagram in SAE J2847-6 Protocol

of operational states for managing WPT, as illustrated in Figure 4.5. The state diagram outlines eight sequential stages that guide the power transfer process.

The first state is the Out of Service state, wherein the EV is not ready for power transfer. This is followed by the Standby state, which is triggered once the EV is plugged in but before communication has been initiated. In the Service Initiation state, a communication link is established between the EV and the charging station, during which configuration data and system parameters are exchanged [62].

The subsequent state, Awaiting Alignment, ensures that the transmitting and receiving coils are properly aligned. If misalignment is detected, an error signal is generated, alerting the user to correct the positioning before proceeding. Once alignment and system conditions are validated, the protocol advances to the Power Transfer Ready state. In this stage, all system parameters are verified and the setup is made ready for energy transfer.

The most critical phase, the Power Transfer Active state, is where actual energy exchange occurs between the charging station and the EV. If any fault or irregularity

arises during this stage—or during the preparation phase—an error signal (E) is triggered, and power transfer is immediately halted to prevent system damage.

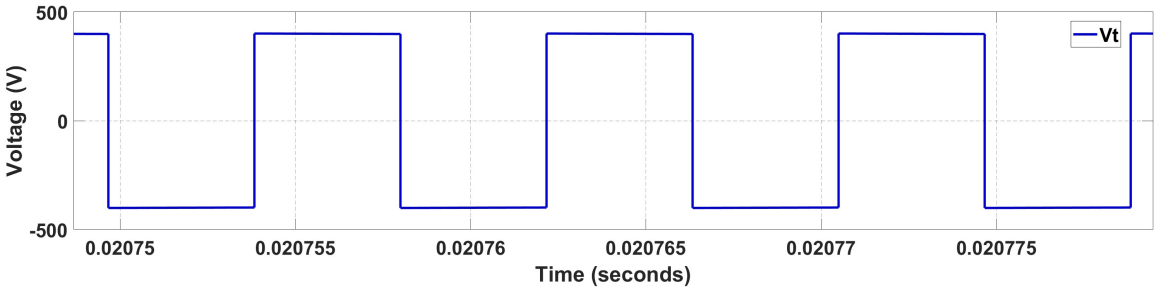
The final state, Service Terminated Occupied, signals the end of the charging session. In this state, all communication links between the EV and the charging station are safely disconnected, completing the WPT cycle.

Communication is a cornerstone of this topology, ensuring synchronized and safe energy transfer. This communication framework can also be extended to EV charging stations that service multiple vehicles simultaneously. For practical implementation, wireless communication protocols such as Wi-Fi may be used to exchange data between the EV and the charging station. Alternatively, CAN based communication provides a more robust and deterministic approach, particularly suited for automotive environments. In either case, a reliable communication channel is essential for the successful operation of the proposed WPT system.

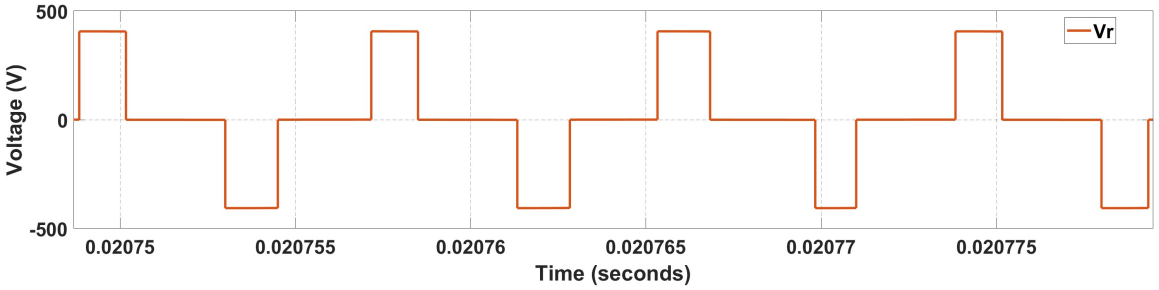
4.5 Result and Discussion

Figure 4.6 illustrates the implementation of the phase shift control technique, which is instrumental in regulating power transfer across both sides of the DAB. A clear phase difference is observed between the transmitting and receiving sides, validating the application of phase shift modulation in the system. This phase displacement is directly influenced by the value of the reference power signal, P_{ref}, which governs the direction and magnitude of energy flow. The control strategy of the DAB converter, as discussed in Chapter 2, is implemented.

By appropriately adjusting P_{ref}, the control algorithm dynamically alters the phase shift between the bridges, thereby enabling bidirectional power flow as required. This approach not only facilitates efficient energy transfer but also ensures that the battery charging process is controlled and optimized. The use of active power reference values



(A) Transmitting Side Voltage



(B) Receiving Side Voltage

FIGURE 4.6: Phase Shift Between Both Sides of DAB

allows for precise modulation of energy delivery, making the control strategy effective for real time power management within the proposed topology.

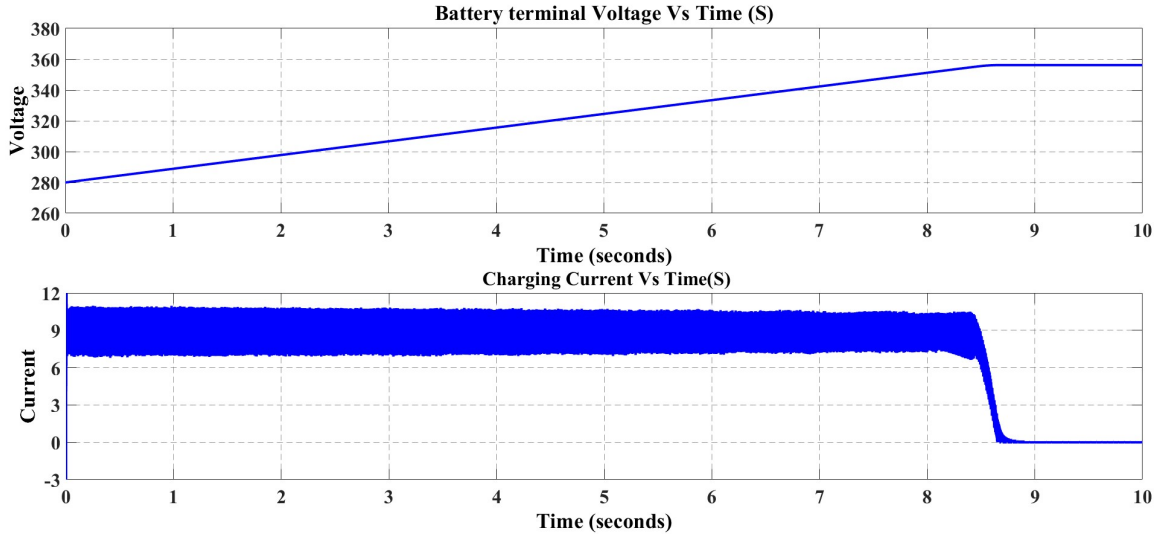


FIGURE 4.7: Battery Terminal Voltage and Current

Figure 4.7 presents the simulation results obtained from a scaled down battery model, where the battery Ah rating has been appropriately reduced to facilitate complete observation of the charging process within the simulation timeframe. The results conform

to the defined battery specifications and clearly demonstrate the charging behavior in both constant voltage (CV) and constant current (CC) modes.

Maintaining stable voltage and current levels during charging is critical to ensure battery safety, longevity, and efficiency. The simulation confirms that the implemented control strategy successfully maintains the required constant voltage and current parameters throughout the charging cycle, thereby validating the effectiveness of the proposed power transfer and control scheme.

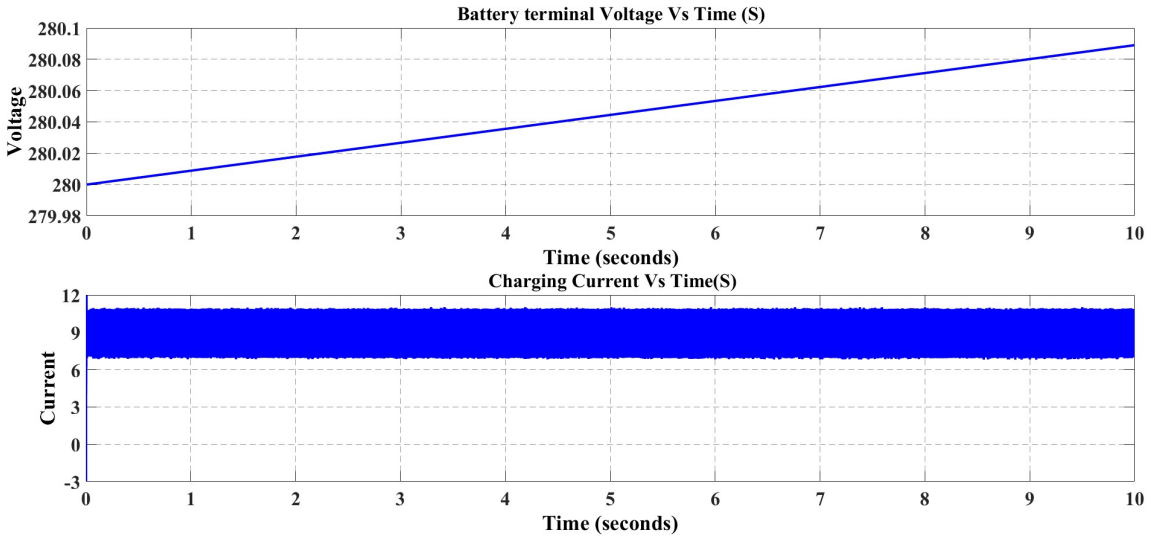


FIGURE 4.8: Actual Charging Voltage and Current of Battery

Figure 4.8 illustrates the charging voltage and current waveforms obtained from the simulation of an actual battery. Due to constraints imposed by the simulation environment, the results represent a shortened duration of the overall charging process. Despite this limitation, the performance of the planar magnetic coils is validated by the observed outcome, confirming their intended functionality.

It is evident that the coefficient of coupling between the coils improves as the physical distance between them decreases. This enhancement in coupling directly contributes to an increase in the overall system efficiency. Accordingly, the simulation results substantiate the effectiveness of employing planar coils in the proposed wireless charging topology, thereby reinforcing the suitability of this approach for practical EV charging applications.

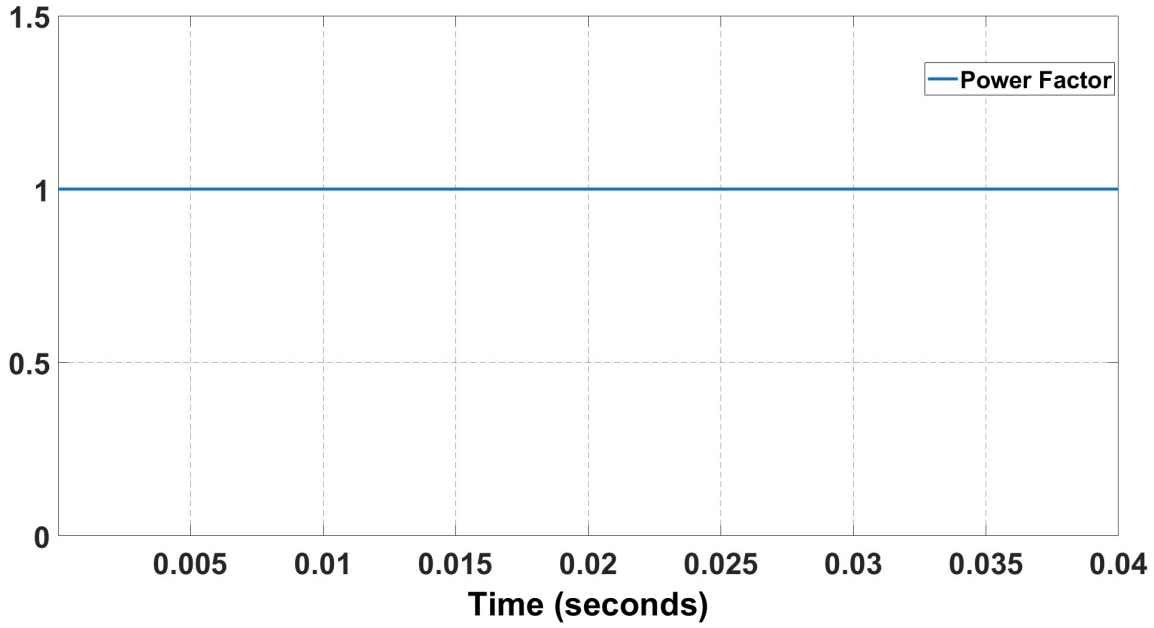


FIGURE 4.9: Power Factor During Power Transmission

Figure 4.9 demonstrates the power factor profile maintained throughout the power transfer process within the system. As observed, the power factor remains consistently close to unity, indicating efficient utilization of input power and minimal reactive power flow. This performance is primarily attributed to the effective operation of the PFC circuit, which plays a critical role in shaping the input current waveform and aligning it with the input voltage.

The ability of the system to sustain a near unity power factor across the entire operating range validates the functionality and design of the proposed topology. These results confirm that the implemented architecture not only supports reliable power transfer but also adheres to power quality standards, thereby ensuring overall system efficiency and compliance.

4.6 Conclusion

The proposed topology successfully combines the benefits of both conductive charging and WPT, offering a hybrid solution that enhances functionality while addressing key safety concerns. By mitigating the risk of electric shock and eliminating safety related

vulnerabilities, the system improves operational reliability. The use of planar magnetic coils enables close physical placement of the transmitting and receiving elements such as in a charging gun configuration which significantly reduces energy losses.

Furthermore, the elimination of mechanical connectors enhances universality, making the proposed design compatible across various EV platforms. The planar coil structure also contributes to increased energy density, which allows for the downsizing of passive compensation components, thereby improving the overall compactness and efficiency of the system. The complete topology was modeled and simulated using MATLAB/Simulink, and the results confirm the feasibility and effectiveness of the proposed solution.

CHAPTER 5

Planar Magnetics based V2V Connector

5.1 Introduction

One effective means of enhancing the adoption of EV technology is through the development of Vehicle to Vehicle (V2V) charging capabilities. V2V charging can be realized using either AC or DC architectures. Conventional V2V AC charging typically depends on the onboard chargers of each vehicle and involves multiple stages of AC-DC and DC AC conversion, leading to increased system complexity and reduced overall efficiency. In contrast, V2V DC charging offers a more streamlined alternative and can be implemented either on-board or off board. In the off board configuration, a dedicated V2V connector facilitates the direct transfer of DC power between vehicles. Figure 5.1 depicts the conventional V2V charging setup, which relies on a DC DC converter to manage power transfer between two EVs [63, 64].

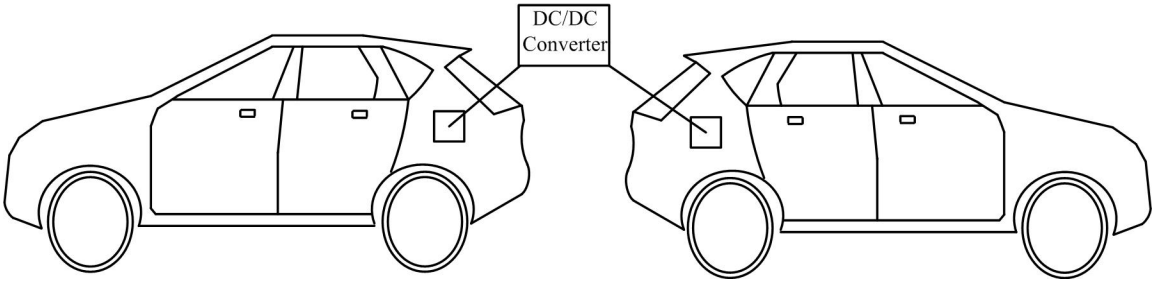


FIGURE 5.1: Conventional Way of V2V Charging

Extensive prior research has addressed various aspects of V2V charging, including the development of bidirectional DC DC converters that enable energy flow in both directions between vehicles. Other studies have proposed multifunctional EV chargers that integrate additional features, such as grid interfacing and energy management. While these advancements have contributed to the growth of V2V capabilities, they often introduce drawbacks such as increased power losses due to multiple conversion stages

and the need for additional components and interfaces, ultimately reducing system efficiency and increasing design complexity [65, 66].

To mitigate these limitations, alternative strategies have been investigated. One such strategy is direct energy transfer, which seeks to minimize conversion losses by enabling direct DC power exchange between EVs. Another approach involves reconfiguring onboard chargers to function as direct DC DC converters, simplifying the architecture but posing challenges in maintaining safety compliance and achieving high energy efficiency [67, 68].

Despite these efforts, existing literature reveals a gap in the development of a unified V2V charging connector that integrates both power and communication functionalities into a single, efficient interface. Although significant progress has been made in V2V power electronics and control strategies, a standardized connector capable of supporting efficient and user friendly V2V energy transfer remains undeveloped [69].

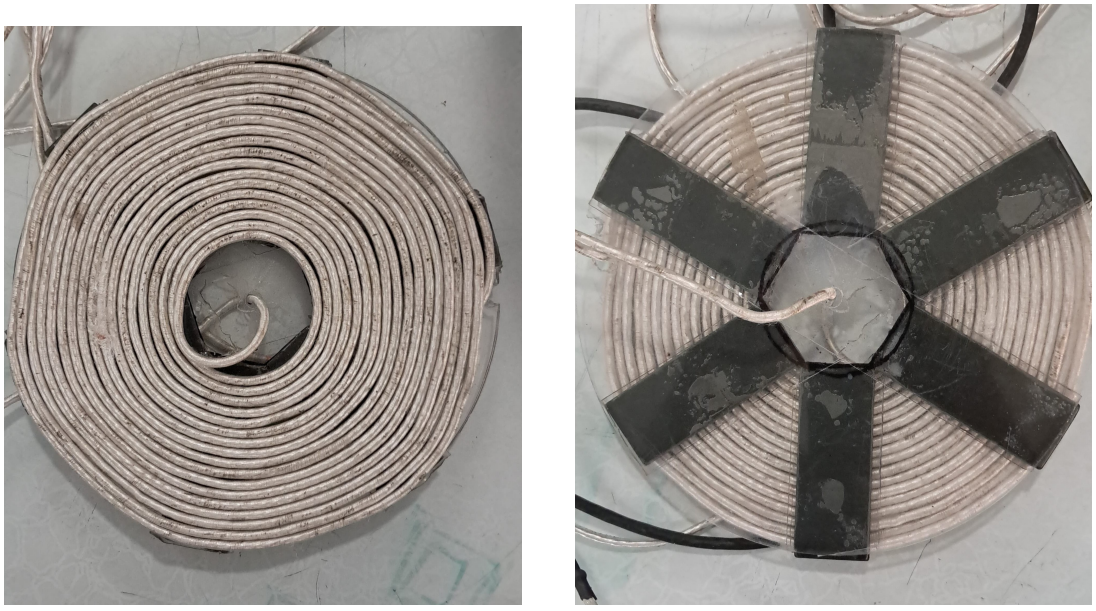
To address this gap, the present work proposes a novel planar magnetics based V2V charging connector. This design aims to streamline the V2V charging process by improving energy transfer efficiency, reducing component count, and embedding communication capabilities directly within the power transfer interface. By leveraging the advantages of planar magnetics, the proposed connector presents a compact, high-performance, and scalable solution for next generation V2V charging infrastructure.

5.2 Proposed Charging Connector

Planar magnetics technology plays a pivotal role in reducing the physical footprint of magnetic components, thereby facilitating the development of more compact and high performance power transfer systems. By operating at higher switching frequencies, planar magnetics effectively minimizes the size of passive components such as inductors and transformers, making it an ideal candidate for integration into modern EV applications where space, efficiency, and thermal management are critical. In contrast, traditional V2V

charging connectors typically rely on bulky DC DC converters that occupy significant volume and add to the system's overall cost and complexity. These limitations underscore the urgent need for a more efficient, scalable, and space conscious connector design.

To address these challenges, the present study explores a novel V2V connector based on planar magnetic technology. The proposed design leverages the inherent advantages of planar structures—including high energy density, low profile, and ease of manufacturing—to streamline the power transfer interface between EVs. This approach not only enhances the overall energy transfer efficiency but also reduces system complexity and cost, thereby improving integration and user experience.



(A) Top Side (B) Bottom Side

FIGURE 5.2: Planar Magnetics Based V2V Connector

Figure 5.2 showcases the hardware prototype of the proposed V2V charging connector. The design features two connection interfaces—each designated for one EV—facilitating direct power exchange between vehicles. The high frequency energy transfer is enabled through a planar magnetic coupling mechanism, which ensures efficient and stable power transmission while maintaining a compact and thermally optimized layout. The close proximity between the magnetic structures improves coupling efficiency, minimizes transmission losses, and allows the connector to operate reliably at higher frequencies.

An essential feature of this design is its enhanced safety profile. The use of planar magnetic coupling inherently eliminates exposed conductive terminals, thereby reducing the risk of electric shock. Furthermore, the system incorporates an electromagnetic self locking mechanism that activates during current flow. This mechanism ensures that the two halves of the connector remain securely attached during the charging process, effectively preventing accidental or unauthorized disconnection. This feature significantly enhances the reliability and integrity of the power transfer process, making it safer and more robust for real world use.

In addition to safety and efficiency, the system's compact design contributes to higher power density, improved thermal management, and reduced material usage. Compared to conventional inductive or wireless charging systems, which often suffer from misalignment sensitivity and lower coupling efficiency, the proposed planar magnetics based connector offers superior performance with reduced alignment constraints. As a result, it presents a practical and scalable solution for future V2V energy transfer systems.

5.3 Communication Protocol

Effective communication is a cornerstone of any V2V charging system, ensuring coordinated operation between the charging and discharging EVs. A robust communication protocol enables real time data exchange, allowing for precise control of power transfer while upholding critical safety and system stability requirements. Through the transmission of essential parameters such as battery state of charge, voltage and current levels, and fault diagnostics, communication ensures interoperability and compatibility between the participating vehicles. The following sections present a detailed implementation of the communication framework used within the V2V charging architecture.

5.3.1 Charging Process

The charging process is initiated by the vehicle that requires energy, which assumes the role of the master. It sends a charging request to the slave vehicle, which then responds by adjusting its output current according to the request. The exchange of control signals and data between the vehicles is facilitated by the CAN protocol, which provides high speed, reliable communication suited for automotive environments. The overall process is divided into three major stages.

Upon pressing the Start button, the master vehicle detects the request for charging. At this point, its Battery Management System (BMS) begins broadcasting battery parameters—such as voltage, state of charge, and temperature—over the CAN bus. The slave vehicle receives this information, verifies compatibility, and subsequently shares its own status. If the system parameters align, the charging authorization is granted. Before initiating power transfer, the system performs crucial safety checks, including insulation resistance measurement and obstruction detection. Only after successful verification of these conditions does charging commence.

Throughout the charging session, the master vehicle's BMS dynamically adjusts the current demand based on battery conditions such as temperature and voltage levels. These updated current requests are sent to the charging EV every 100 milliseconds via the CAN bus. Simultaneously, both vehicles' BMS continuously monitor operational parameters to ensure system stability and detect faults in real time. In the event of any irregularities—such as communication failure, voltage mismatch, or overcurrent—the power delivery is immediately and safely interrupted.

Upon reaching the predefined charging completion condition, the master vehicle initiates a controlled ramp down of the current to zero, signaling the end of power transfer. The slave vehicle confirms the cessation of output before terminating the session. The charging process may also be halted manually via an Emergency Stop button or automatically in the presence of faults such as invalid parameter ranges, protocol errors,

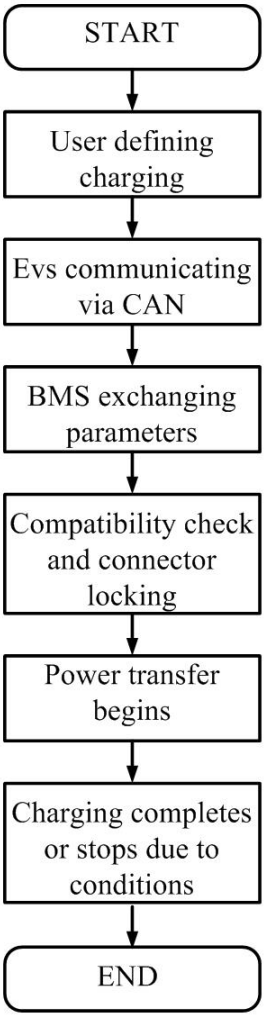


FIGURE 5.3: Flowchart for Charging and Discharging Process

or timeout violations. In all cases, the shutdown is executed in a gradual and secure manner to protect both the hardware and battery integrity.

5.3.2 Discharging Process

The discharging sequence operates similarly to the charging process, with the primary difference being the reversal of roles: the EV supplying power acts as the master, while the receiving EV becomes the slave. This configuration supports the controlled delivery

of energy either to another vehicle, an external DC load, or the power grid in bidirectional charging scenarios.

Once the discharging request is initiated, the master EV's BMS exchanges operational parameters with the slave system to evaluate compatibility. If the received data meets the required thresholds, the V2V connector is securely locked in place, and pre discharge safety checks—including insulation testing and voltage validation—are conducted. Upon successful validation, power transfer is initiated.

During discharging, the BMS continuously monitors the system to prevent over depletion of the energy source. Real time adjustments to current output are made in response to system dynamics such as battery voltage and load conditions. An HMI is provided for real time control and feedback, allowing the user or control algorithm to emulate variable power demands and adapt accordingly.

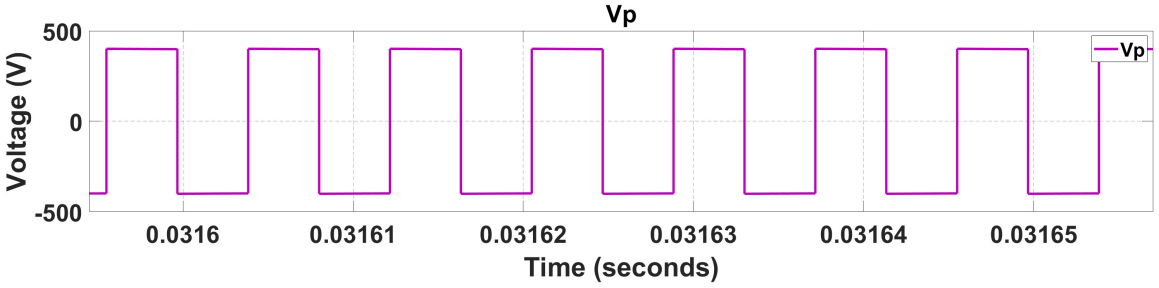
As the energy transfer nears completion, the discharging current is progressively reduced to zero to facilitate a controlled shutdown. Discharging is terminated upon meeting preset conditions such as energy threshold limits, manual commands, or detection of anomalies within the system. Similar to the charging phase, this sequence ensures safety, efficiency, and prolonged battery life.

5.4 Result and Discussion

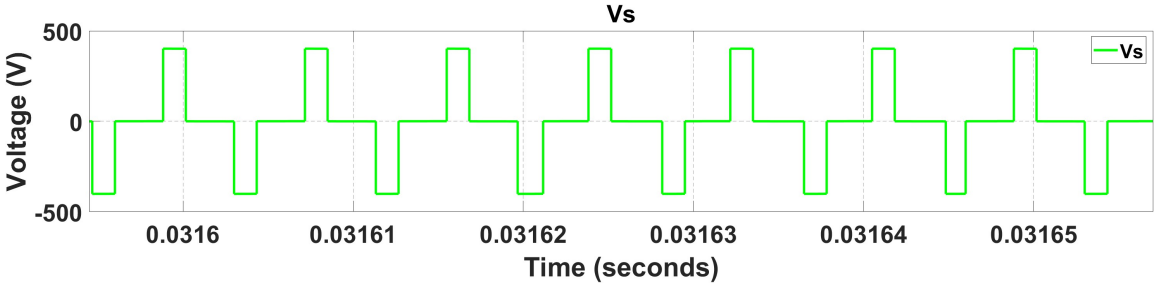
To assess the effectiveness of the proposed planar magnetics based connector, a 3.3kW V2V charging system was modeled and simulated using MATLAB/Simulink. The simulation framework was designed to evaluate the connector's ability to support efficient and reliable energy transfer between EVs. For functional validation, the simulation was initially configured with the actual battery ampere hour (Ah) rating. However, due to computational limitations inherent to the simulation environment, the battery capacity was scaled down to a lower Ah value. This modification enabled the visualization of a complete charging cycle within a manageable simulation duration, without compromising

the accuracy of the system's dynamic behavior. The control strategy of the DAB converter, as discussed in Chapter 2, is implemented.

Despite this reduction, the simulation results successfully captured the essential characteristics of the charging process, including current regulation, voltage behavior, and system response under load. The findings confirm the practicality and efficiency of the planar magnetics based connector, demonstrating its capability to facilitate seamless and controlled V2V energy transfer under realistic operating conditions.



(A) Voltage on EV 1 Side of Connector



(B) Voltage on EV 2 Side of Connector

FIGURE 5.4: Voltages on Both Side of Connector

Figure 5.4 depicts the phase shift behavior at both ends of the planar magnetics based connector during the V2V charging process. In this configuration, EV 1 operates as the power source, supplying energy to EV 2. This is achieved by appropriately configuring the active power reference parameter (P_{ref}) to regulate the magnitude and direction of power flow. The waveform demonstrates a clearly defined and stable phase displacement between the transmitting and receiving sides, confirming synchronized operation of the DAB control mechanism.

The observed results validate the system's ability to establish a consistent and controlled power exchange between the two EVs. This substantiates the functional

effectiveness of the proposed connector and control strategy in enabling efficient and reliable V2V energy transfer.

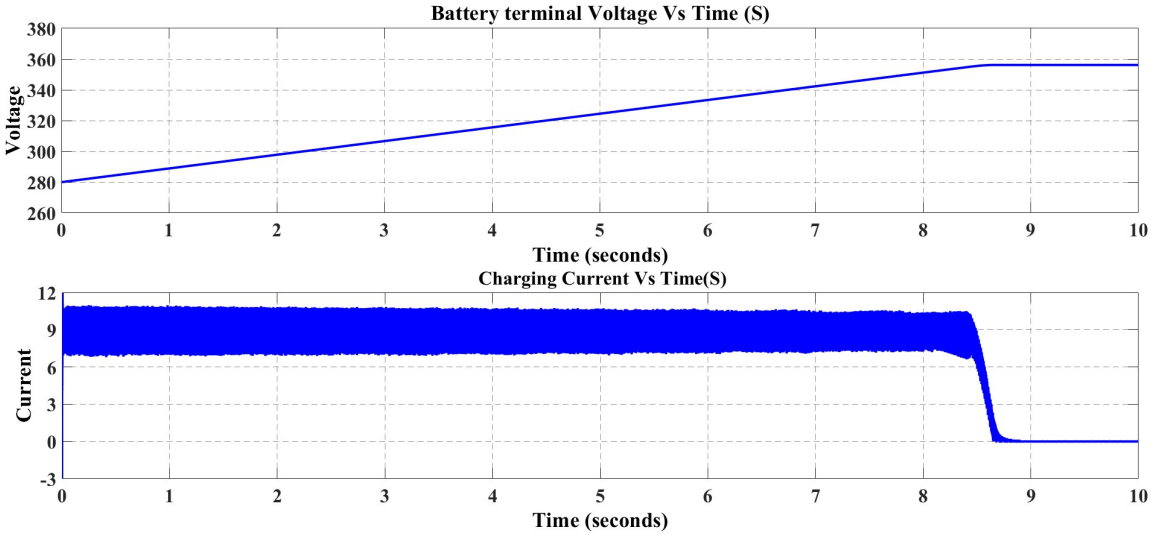


FIGURE 5.5: Battery Terminal Voltage and Current When EV 1 Charging EV 2 at Reduced Ah

Figure 5.5 illustrates the simulated V2V charging process between two EVs. In this configuration, EV 1 operates as the source, discharging its battery, while EV 2 functions as the receiver, undergoing the charging process. To ensure the visualization of a complete charge cycle within a practical simulation window, the battery model used for EV 2 was configured with a reduced ampere hour (Ah) capacity.

As shown in the figure, once the battery reaches its predefined charge threshold, the system autonomously terminates the charging sequence. This behavior confirms the correct implementation of the underlying communication and control protocols, ensuring seamless coordination and safe operation between the two EVs during energy transfer.

5.4.1 EV 2 Charging EV 1

Figure 5.6 illustrates the phase shift observed between the primary and secondary sides of the DAB converter during operation. The presence of a controlled and stable phase displacement confirms the effectiveness of the bidirectional power transfer mechanism employed in the system. The waveform clearly demonstrates a consistent phase offset,

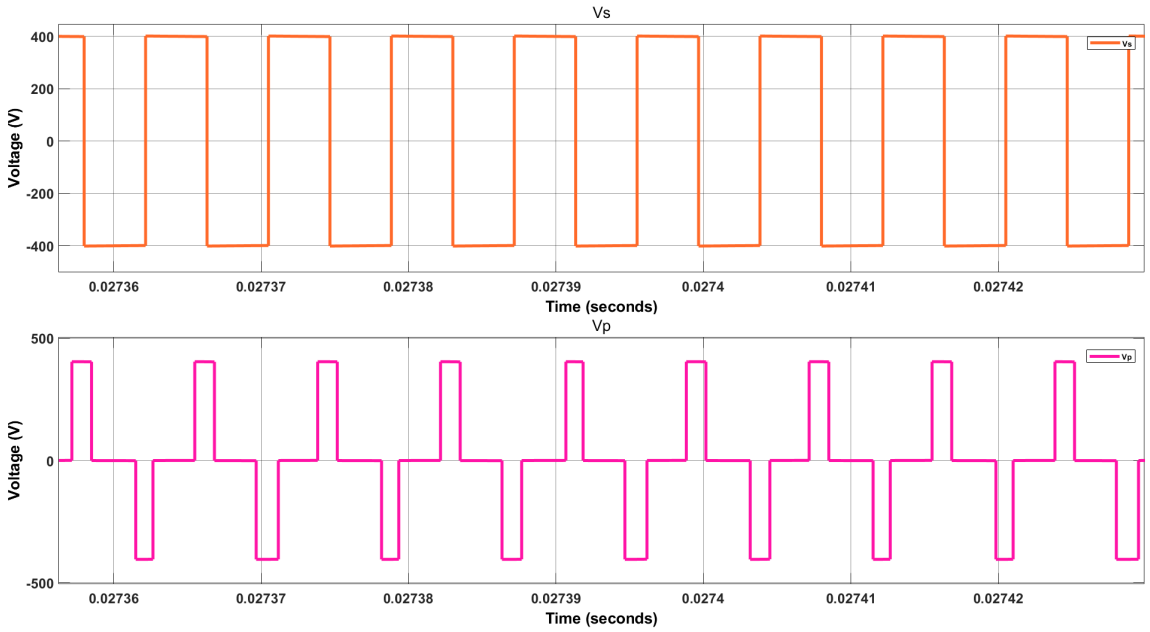


FIGURE 5.6: Phase Shift of DAB During Charging of EV 2

which aligns well with the theoretical behavior expected from phase shift modulation techniques.

This consistent phase relationship verifies that the power transfer between the two EVs is being carried out in a regulated and efficient manner, without introducing significant waveform distortion. These results validate the integrity of the modulation and control strategy implemented within the DAB topology.

Figure 5.7 presents the voltage and current waveforms at the battery terminals of EV 1 during its charging cycle. As shown, the battery voltage gradually rises over time, consistent with expected behavior in a well regulated charging environment. Throughout most of the charging period, the current remains relatively constant, indicating operation in constant current (CC) mode, which ensures a uniform and controlled energy flow into the battery.

Towards the end of the charging cycle, a noticeable decrease in current is observed, signifying a transition from CC mode to constant voltage (CV) mode. This shift is characteristic of standard battery charging protocols, where the charging system prioritizes voltage regulation as the battery approaches full capacity. The waveform thus

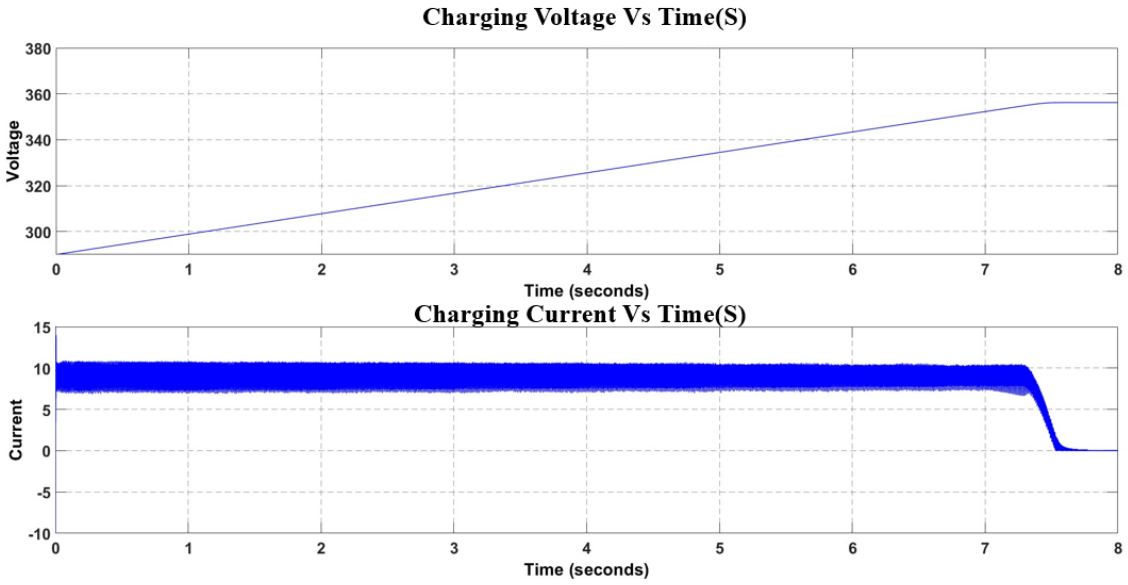


FIGURE 5.7: Battery Terminal Voltage and Current When EV 2 Charging EV 1 at Reduced Ah

confirms the correct implementation of charging control strategies within the proposed system.

5.5 Conclusion

This study presented a novel V2V charging connector architecture based on planar magnetics, aimed at overcoming the limitations of conventional V2V energy transfer systems. The proposed system was extensively simulated using MATLAB/Simulink, and the results demonstrated performance consistent with theoretical expectations. The charging operation was executed smoothly, maintaining the stability of all system components throughout the process.

Additionally, the integrated communication framework functioned effectively, enabling real time coordination between the two EVs and ensuring accurate control of power flow. The compact structure of the connector, combined with the minimal spacing between transmitting and receiving coils, contributed to high energy transfer efficiency by significantly reducing coupling losses.

Overall, the successful integration of power transfer and communication functionalities validates the practicality and robustness of the proposed connector. It offers a scalable and efficient solution for next generation V2V charging systems, making it well suited for real world deployment in emerging EV infrastructures.

CHAPTER 6

Conclusion and Future Scope

This thesis presents a unified exploration of planar magnetics as an enabling technology across three distinct but interrelated domains of electric vehicle (EV) power systems: onboard charging with integrated auxiliary supply, non-conductive charging interface design, and vehicle-to-vehicle (V2V) power transfer mechanisms. Each chapter investigates a key challenge in the existing EV infrastructure and demonstrates how planar magnetic components, combined with effective control strategies such as dual active bridge (DAB) phase-shift modulation, offer scalable, efficient, and compact solutions.

In the first domain, the integration of a tertiary planar winding within a high-frequency transformer enables direct auxiliary battery charging from the onboard charger, thereby eliminating the need for a separate Auxiliary Power Module (APM). This significantly reduces system complexity and enhances power density while maintaining safe and consistent voltage delivery under varying operating modes.

The second contribution involves the conceptualization of a non-conductive EV charging gun that merges the safety benefits of wireless power transfer with the efficiency of planar magnetics. By utilizing closely-coupled planar coils and simplified alignment requirements, the proposed design addresses challenges such as electric shock hazards, connector incompatibility, and power transfer efficiency, all while supporting communication protocols like SAE J2847 for secure charge authorization.

The final chapter proposes a planar magnetics-based V2V connector, demonstrating its feasibility through simulation and validation. The connector incorporates both power transfer and communication layers in a single compact module, supporting bidirectional energy exchange between EVs without the need for intermediary DC-DC converters. This advancement directly addresses range anxiety and promotes decentralized, peer-assisted energy management within EV networks.

Future Scope

While the simulations and theoretical validations affirm the technical soundness of the proposed designs, practical deployment necessitates further research in the following areas:

- **Hardware Implementation and Prototyping:** Full-scale hardware realization of the three systems will be essential to assess real-world performance, thermal management, electromagnetic interference, and durability under varying load and environmental conditions.
- **Power Scalability and Thermal Optimization:** Future work can focus on increasing the power rating beyond 3.3 kW while maintaining high efficiency. This includes improved magnetic core materials, thermal packaging techniques, and optimized coil geometries for planar implementations.
- **Standardization and Interoperability:** To ensure broad adoption, the proposed systems must be tested against existing standards such as ISO 15118 and SAE J2847. Compatibility with different EV platforms and regional regulatory norms is a necessary evolution of the current designs.
- **Extended Communication Integration:** More robust, real-time bidirectional communication—possibly integrating Vehicle-to-Grid (V2G) protocols—could make these systems more responsive and adaptive in dynamic grid or peer-to-peer environments.

Overall, the thesis lays the groundwork for a new class of integrated EV power interfaces centered on planar magnetic technology, demonstrating their potential to simplify system architecture, reduce form factor, and increase charging efficiency.

ANNEXURE A

DESIGN AND DEVELOPMENT OF POWER SUPPLY FOR BIOMEDICAL APPLICATIONS

A.1.1 Literature Survey

In modern healthcare, ensuring efficient and reliable power management is essential for the operation of biomedical devices. Among various DC-DC converters, isolated converters play a crucial role in medical electronics by providing electrical separation between different circuits. This isolation is particularly vital in sensitive biomedical systems, where it acts as a protective barrier between power circuits and signal pathways, ensuring patient safety and device accuracy.

The significance of isolation in biomedical applications stems from its multiple advantages. Firstly, it helps in suppressing common-mode electromagnetic interference (EMI), which is critical for maintaining signal integrity in diagnostic and monitoring equipment. Additionally, isolation transformers can be engineered to enhance converter efficiency, optimizing energy transfer for medical instruments. Furthermore, multiple winding configurations can be incorporated into the system design to support additional functionalities, making isolated converters adaptable for complex medical environments [70, 71].

Isolated converters are typically derived from non-isolated topologies, with some originating from buck-derived designs while others follow buck-boost structures. Among these, buck-derived isolated converters often face challenges related to power quality and signal stability, prompting the widespread adoption of buck-boost isolated converters in biomedical applications [72, 73].

Among various buck-boost isolated converter topologies, the flyback converter has emerged as a preferred solution due to its simplicity and efficiency. Unlike other isolated

designs, the flyback converter requires only one switch and one diode, significantly reducing component count while maintaining reliable performance. This reduced complexity makes it a highly practical choice for biomedical devices that require compact and cost-effective solutions. Additionally, the flyback converter is well-suited for applications demanding multiple input or output configurations, making it invaluable in medical equipment that requires flexible power delivery across multiple channels [74, 75].

Given its advantages, the flyback converter continues to gain traction in biomedical power management systems, ensuring precise and stable energy transfer while preserving circuit isolation [76, 77].

To achieve multiple regulated outputs in biomedical systems, several existing power conversion techniques have been explored. A widely adopted method is the use of independent low-dropout (LDO) regulators, commonly referred to as the multiple-LDO strategy. This approach ensures low ripple and noise performance, making it suitable for biomedical applications. However, the efficiency of LDO regulators is significantly lower compared to switching regulators, particularly when handling multiple voltage domains [78, 79].

An alternative approach is the use of independent switching DC-DC converters. These converters improve efficiency by utilizing inductive energy storage to regulate different voltage levels. While this method enhances power conversion efficiency, it leads to increased system complexity, PCB footprint, and cost due to the requirement of multiple inductors and control circuits [80, 81].

To address the limitations of traditional approaches, single-inductor multiple-output (SIMO) converters have been introduced. These converters replace multiple single-output switching regulators with a single-inductor topology, improving space efficiency. However, a major challenge associated with SIMO converters is cross-regulation (CR), where variations in load current on one channel affect the stability of other outputs. Additionally, the nature of SIMO operation results in large voltage ripples, which are difficult to mitigate even with increased output capacitance. These drawbacks hinder their

suitability for biomedical applications that demand stringent voltage stability and low ripple characteristics [82, 83].

Furthermore, since biomedical systems generally operate under light load conditions, switching converters, which are more efficient at heavier loads, may not always provide the best solution. Other available power supplies are designed primarily for implantable medical devices, making them unsuitable for this application due to the different power requirements and operational constraints [84, 85].

In summary, while multiple-LDO strategies offer low noise and ripple performance, their efficiency is limited. Independent switching DC-DC converters improve efficiency but increase complexity and cost. SIMO converters offer space efficiency but face challenges with cross-regulation and voltage ripple. Therefore, selecting the appropriate power conversion technique for biomedical systems requires careful consideration of efficiency, complexity, and the specific requirements of the application [86, 87].

In modern healthcare, wireless power transfer technology plays a crucial role in enhancing implantable medical devices by enabling efficient and seamless energy delivery without the need for bulky batteries or frequent replacements. These implants, such as pacemakers and neurostimulators, benefit from wireless energy transmission, ensuring uninterrupted functionality while minimizing the risks associated with invasive procedures for battery changes. However, traditional biomedical devices, including diagnostic and therapeutic equipment, continue to rely on conventional wired or battery-powered solutions to maintain stability and precision in medical applications. Considering the complexities of biomedical applications, it is essential to develop optimized power supply solutions that not only deliver high efficiency but also minimize ripple and cross-regulation effects. These factors are crucial to ensure the stable and reliable operation of medical devices, where fluctuations in power can directly impact performance and patient safety. Moreover, the compact design requirement adds another layer of challenge, as biomedical devices often have stringent size constraints that limit bulky power supply components [88, 89].

In addition to power efficiency, a robust and precise communication mechanism is necessary to facilitate controlled power transfer. This ensures that the device receives the exact amount of power required, preventing issues such as overcharging or inconsistent energy delivery. Reliable power communication plays a vital role in maintaining the integrity of biomedical instruments, preventing potential disruptions in monitoring or therapeutic processes.

A.1.2 Problem Statement

There is a ECG monitor which is operating in different modes of operation as specified in Table A.1.1. To accommodate these varying power demands effectively, this thesis presents the design and development of a flyback converter integrated with a USB Power Delivery (USB PD) interface. The proposed converter is engineered to dynamically regulate its output according to the ECG monitor's mode selection, thereby ensuring precise and reliable power delivery while maintaining electrical isolation. By utilizing the flyback topology, the system is capable of seamlessly transitioning between different voltage levels—ranging from 5V to 20V—while consistently supplying a stable 3A current.

TABLE A.1.1: Power Requirement in Different Modes

Modes	***Specification***
Mode I	20V, 3A
Mode II	15V,3A
Mode III	9V, 3A
Mode IV	5V, 3A

This approach enhances the adaptability and efficiency of biomedical power management while contributing to a compact and cost-effective solution suitable for medical applications.The proposed system leverages USB PD 3.0 communication to provide multiple output configurations, allowing seamless integration with an ECG monitor. This approach ensures efficient power management while maintaining minimal

losses in transmission. By utilizing USB PD technology, the charger is capable of adapting to different voltage levels required by the ECG monitor, further improving energy utilization and device longevity. Figure A.1.1 represents a pictorial representation of the USB PD charger for ECG monitor.

FIGURE A.1.1: Power Supply for a ECG Monitor

A.1.3 Objective of Thesis

The primary objective of this thesis is to design and develop a flyback converter integrated with a USB Power Delivery (USB PD) interface for biomedical applications. Specifically, the system aims to facilitate efficient power management for an ECG monitor that operates in multiple modes, ensuring seamless communication between the device and the power supply using USB PD technology. By enabling dynamic voltage adjustments, the proposed converter will enhance flexibility, efficiency, and reliability in medical device power delivery.

To achieve this objective, the following key goals have been outlined:

- **Design and Development of the Flyback Converter:** Develop a flyback converter capable of delivering multiple voltage levels as required by the biomedical load.

The converter should ensure stable and efficient power transfer while maintaining compactness and cost-effectiveness.

- **Integration with USB PD Interface:** Establish a robust communication link between the flyback converter and the USB PD protocol, enabling the ECG monitor to request specific voltage levels based on operational requirements. This process will involve implementing appropriate control mechanisms to facilitate accurate power negotiation.

- **Testing and Validation Under Various Conditions:** Conduct comprehensive testing of the designed charger under different operating scenarios, including varying load demands, fault conditions, and system disturbances. This validation process will ensure reliable performance and adherence to medical safety standards.

- **Practical Implementation in a Biomedical Application:** Successfully integrate the developed flyback converter within a biomedical system, demonstrating its ability to provide optimized power delivery while maintaining electrical isolation and compliance with medical-grade specifications.

Through this research, the thesis aims to contribute to advancements in biomedical power management systems by leveraging USB PD technology for precise and efficient energy transfer.

A.1.4 Outline of Annexure

The Annexure is organized as follows:

- **Chapter A2: Flyback Converter**
  This chapter provides a comprehensive overview of the fundamental principles of the flyback converter, including its operating modes and relevance to the intended biomedical application.

- **Chapter A3: USB Power Delivery (PD) Technology**

  This chapter examines the USB Power Delivery (PD) technology utilized for efficient communication between the flyback converter and the ECG monitor, ensuring precise power transfer in accordance with the device's requirements.

- **Chapter A4: Flyback Converter Design**

  This chapter presents a detailed discussion of the design methodology of the flyback converter, highlighting key parameters, component selection, and system architecture tailored for biomedical applications.

- **Chapter A5: Results and Discussion**

  This chapter analyzes the experimental results obtained from the hardware prototype, providing an in-depth discussion on the performance evaluation, validation, and implications of the implemented design.

- **Chapter A6: Conclusion**

  This chapter summarizes the key findings of the research, highlighting the contributions made toward improving biomedical power management and addressing the challenges encountered during the design and implementation process.

- **Chapter A7: Future Scope**

  This chapter outlines potential future research directions, proposing enhancements and advancements that could further optimize the flyback converter design for biomedical applications.

FLYBACK CONVERTER

A.2.1 Introduction

The flyback converter is a widely adopted isolated DC-DC converter topology, favored for its simplicity, cost-effectiveness, and high efficiency in the power range of 10–100 W. It is particularly well-suited for applications requiring electrical isolation and compact design, such as consumer electronics, industrial control systems, and medical equipment. For instance, in medical power supplies where a regulated 60 W output is often required, the flyback converter offers an ideal balance of performance, reliability, and size.

Unlike other isolated topologies, the flyback converter uses a coupled inductor or transformer not only for voltage transformation and isolation but also to store energy during the switch-on period and release it during the switch-off period. This dual functionality eliminates the need for a separate output inductor, simplifying the overall circuit design. Additionally, it can efficiently accommodate multiple output rails from a single transformer, making it attractive in systems with diverse voltage requirements.

To place the flyback converter in context, Table A.2.1 presents a comparative overview of commonly used isolated converter topologies such as forward, push pull, and half-bridge converters. The table outlines their structural differences, number of components, key features, and respective disadvantages. This comparison highlights why the flyback topology is particularly advantageous in low to medium power applications where simplicity and isolation are critical.

The flyback converter is conceptually derived from the conventional buck boost converter, evolving through a series of structural modifications that enhance its functionality and applicability in isolated power supply systems. As shown in Figure. A.2.1a, the basic buck-boost topology consists of a single inductor (L), a switch (Q), a diode (D), and an output capacitor (C), delivering an inverted and regulated output

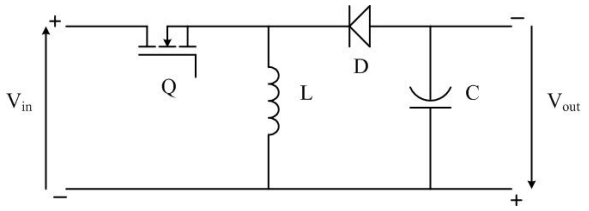
TABLE A.2.1: Comparison of Isolated Converter Topologies

Name	Derived from	Number of Components	Features	Disadvantages
Forward Converter	Buck Converter	1S, 3D, 1L, 1C, 1T	• Power flow is unidirectional (i.e., from source to sink). • High energy efficiency with good power rating.	• Core of high-frequency transformer is underutilized. • Only one output with same polarity as input.
Push-Pull Converter	Buck Converter	2S, 2D, 1L, 1C, 1T (center tapped)	• Better core utilization; magnetized in both directions. • Higher efficiency; suitable for high power applications.	• Flux walking phenomenon. • Poor primary-secondary coupling causes leakage flux. • Requires high rating switches.
Half-Bridge Converter	Buck Converter	2S, 2D, 1L, 1C, 1T (center tapped)	• Core magnetization in both directions. • Reduced flux walking phenomenon.	• High switch current due to topology.
Flyback Converter	Buck-Boost Converter	1S, 1D, 1C, 1T	• High input voltage range. • Efficient for low to medium power applications.	• High voltage stress across components. • Limited power handling capability.

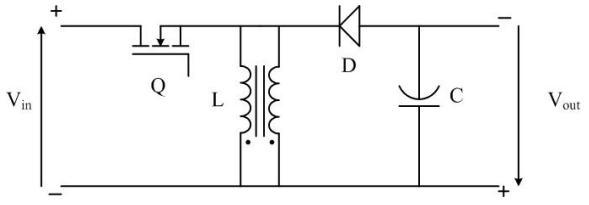
voltage. However, this topology lacks galvanic isolation, which is a critical requirement in applications such as medical instrumentation and safety-critical systems.

To address this limitation, the inductor is replaced with a coupled inductor or transformer, as illustrated in Figure. A.2.1b, enabling energy storage during the switch-on period and its transfer to the output during the switch-off period. This progression continues in Figure. A.2.1c, where the transformer is explicitly modeled with primary and secondary windings (N_P and N_S), establishing the foundation of the flyback converter. The circuit now ensures electrical isolation while preserving the energy transfer principle of the buck-boost topology.

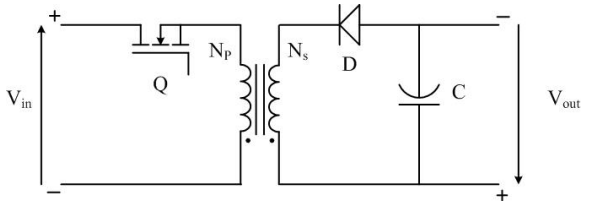
Further modifications, shown in Figs. A.2.1d and A.2.1e, include variations in switch and diode placement, as well as winding orientation. These changes enable the converter to provide either positive or negative output polarity with respect to ground, depending on the



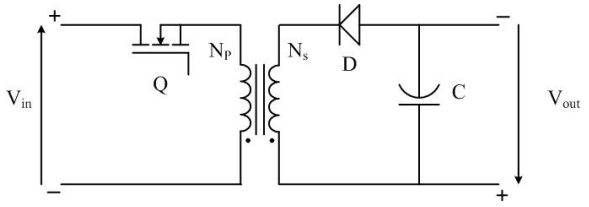
(A) Buck-Boost



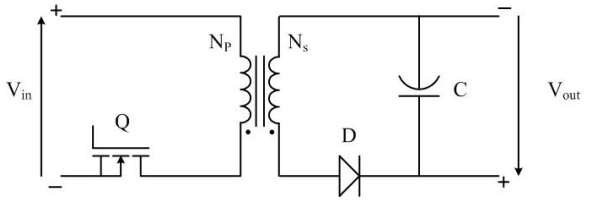
(B) Coupled Inductor



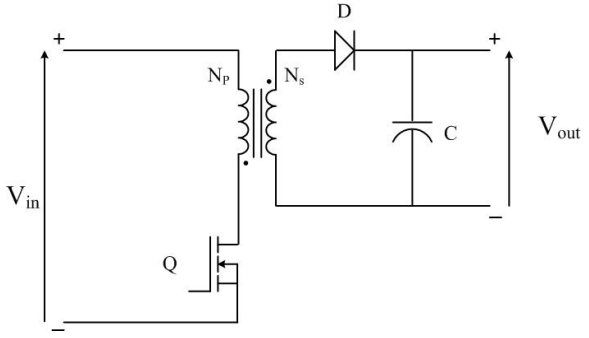
(C) Isolated Flyback



(D) Variant A



(E) Variant B

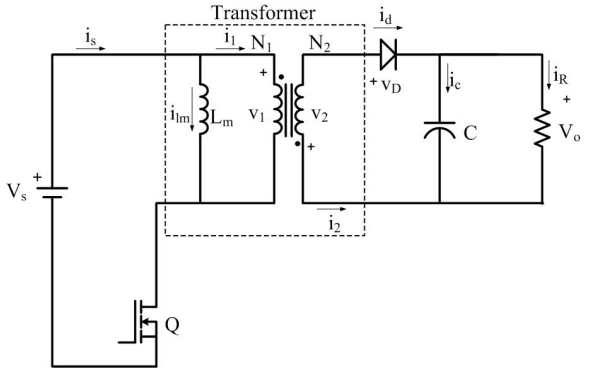


(F) Final Flyback Converter

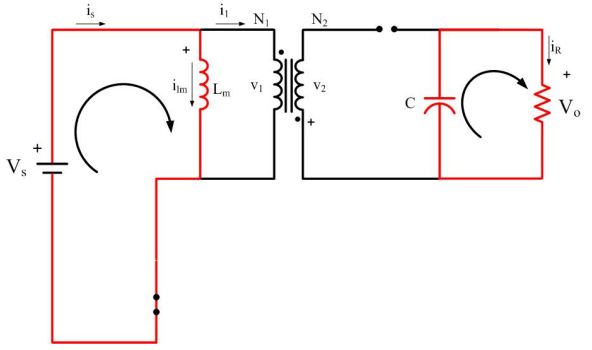
FIGURE A.2.1: Step by Step Derivation of Flyback Converter from Buck Boost Topology

application requirements. Additionally, the use of a transformer allows for voltage scaling through the turns ratio, supporting both step-up and step-down conversion in a single stage.

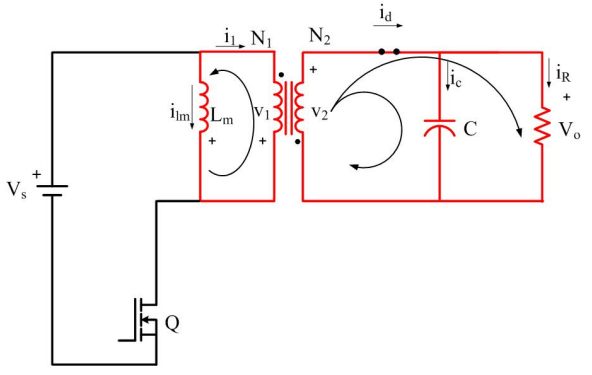
This evolutionary path from the buck-boost to the flyback converter not only introduces galvanic isolation but also improves safety, design flexibility, and adaptability to a wide range of power levels. These advantages make the flyback converter highly suitable for low to medium power isolated DC-DC conversion [90].



(A) Circuit Diagram



(B) Mode I: Switch ON



(C) Mode II: Switch OFF

FIGURE A.2.2: Basic Flyback Converter Circuit and its Operation Modes

The flyback converter is a widely used isolated DC-DC converter topology that stores energy in the magnetic field of the transformer during the switch-on period and transfers it to the load during the switch-off period. As shown in Figure. A.2.2a, the circuit consists of a primary-side switch (Q), transformer with magnetizing inductance (L_m), a diode (D), and output capacitor (C). Following is the analysis of the converter in mode I, as shown in Figure A.2.2b. The analysis of the flyback converter in the mode I is as follows, i_1,i_2 are the currents flowing in the primary and secondary side of the flyback transformer respectively. V_S is the source voltage and V_O is the output voltage of flyback converter. Figure A.2.2 represents the flyback converter when operating in both modes. Analysis is mode I is follows,

$$i_2 = 0 \tag{1}$$

$$i_1 = 0 \tag{2}$$

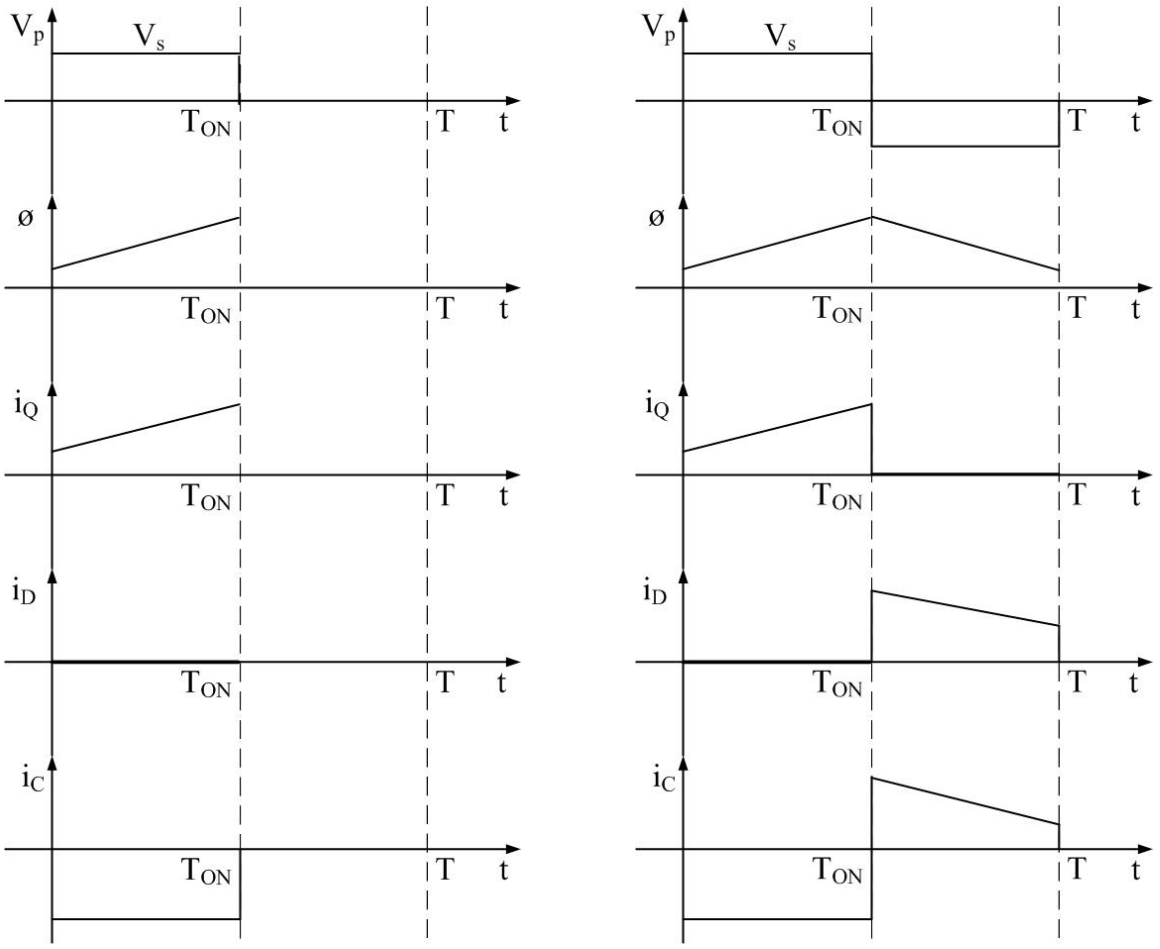
$$V_2 = V_1 \left(\frac{N_2}{N_1}\right) = V_s \left(\frac{N_2}{N_1}\right) \tag{3}$$

$$V_D = -V_0 - V_S \left(\frac{N_2}{N_1}\right) < 0 \tag{4}$$

$$v_1 = v_s = L_m \frac{di_{lm}}{dt} \tag{5}$$

$$\frac{di_{lm}}{dt} = \frac{\Delta i_{lm}}{\Delta t} = \frac{\Delta i_{lm}}{DT} = \frac{V_s}{L_m} \tag{6}$$

$$(i_{lm})_{\text{closed}} = \frac{V_s DT}{L_m} \tag{7}$$



(A) Mode I (B) Mode II

FIGURE A.2.3: Waveform for Overall Flyback Operation

During the first interval (Mode I, Figure. A.2.2b), when the switch is ON, current flows through the primary winding, and energy is stored in the transformer's core as magnetic energy. During this time, the secondary diode is reverse-biased and isolates the load. In the second interval (Mode II, Figure. A.2.2c), the switch is turned OFF, and the collapsing magnetic field induces a voltage across the secondary winding, forward-biasing the diode. This allows the stored energy to transfer to the output capacitor and load. Figure B.2.2 represents the waveform for operation of flyback converter. Analysis of the flyback converter in Mode II is as follows,

$$v_1 = -V_0 \left(\frac{N_1}{N_2}\right) \tag{8}$$

$$v_2 = -V_0 \tag{9}$$

$$V_1 = V_2 \left(\frac{N_1}{N_2}\right) = -V_0 \left(\frac{N_1}{N_2}\right) \tag{10}$$

$$v_1 = L_m \frac{di_{lm}}{dt} = -V_0 \left(\frac{N_1}{N_2}\right) \tag{11}$$

$$\frac{di_{lm}}{dt} = \frac{\Delta i_{lm}}{\Delta t} = \frac{\Delta i_{lm}}{(1-D)T} = \frac{-V_0}{L_m} \left(\frac{N_1}{N_2}\right) \tag{12}$$

$$(i_{lm})_{\text{open}} = \frac{-V_0(1-D)T}{L_m} \left(\frac{N_1}{N_2}\right) \tag{13}$$

$$(i_{lm})_{\text{closed}} + (i_{lm})_{\text{open}} = 0 \tag{14}$$

$$\frac{V_S DT}{L_m} - \frac{V_0(1-D)T}{L_m} \left(\frac{N_1}{N_2}\right) = 0 \tag{15}$$

$$V_0 = V_S \left(\frac{D}{1-D}\right) \left(\frac{N_2}{N_1}\right) \tag{16}$$

Equation 16 illustrates the final equation for the flyback converter [90]. This cyclical storage and transfer of energy enables voltage step-up or step down along with galvanic isolation, making the flyback converter suitable for low to medium power applications [91].

The following section explores the modes of operation of the flyback converter, with particular focus on the behavior of circuit components during the switch on and switch off intervals, which fundamentally govern its performance and efficiency.

A.2.1.1 CCM Mode of Operation

In Continuous Conduction Mode (CCM), the flyback converter operates with a distinct current waveform and energy transfer mechanism compared to Discontinuous Conduction Mode (DCM). When the MOSFET is switched on, the current in the primary winding ramps up from a non-zero offset. This offset is due to residual energy continuously maintained in the transformer core, which prevents the current from falling to zero between cycles. Upon switching off the MOSFET, energy stored in the transformer is transferred to the secondary side, where the current begins to ramp down. However, it does not reach zero before the next switching cycle begins, resulting in continuous current conduction. Consequently, the current waveform on both the primary and secondary sides assumes a trapezoidal shape—often described as a "ramp on a step." Figure A.2.4 depicts

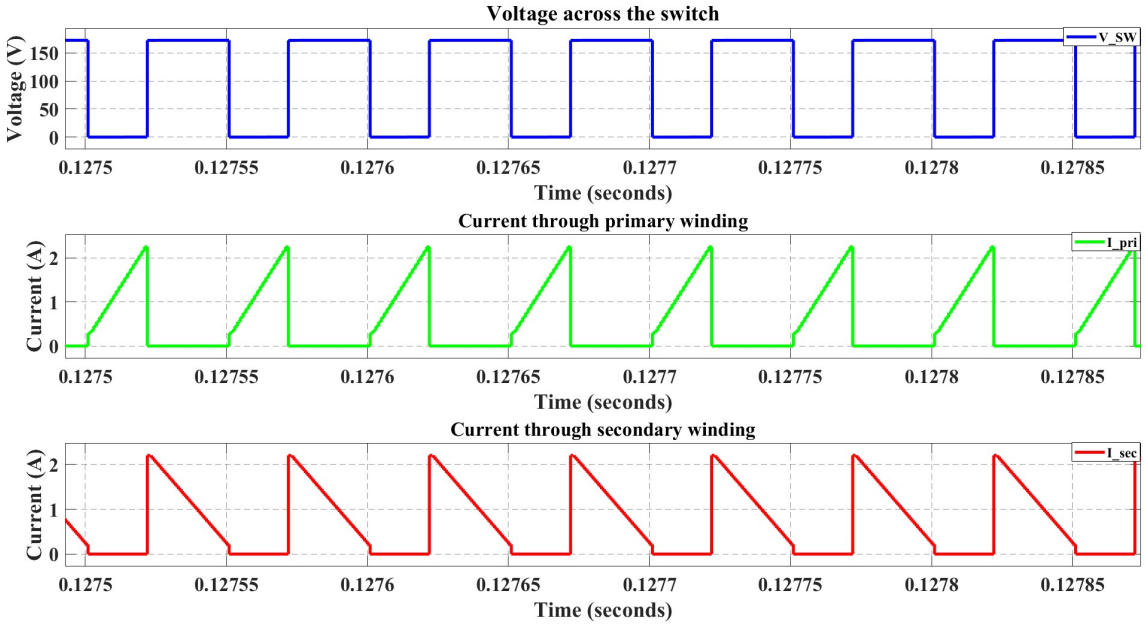


FIGURE A.2.4: Waveform for CCM Mode of Operation

the output of the flyback converter in CCM mode of operation. A key feature of CCM is the absence of dead time: there is always current flowing through either the primary or secondary winding, but never simultaneously through the MOSFET and the output diode. As load demand decreases, the residual energy—or the flat portion of the current waveform—diminishes, while the ramp component remains the design focus. Unlike

DCM, ripple currents in CCM are smaller, reducing RMS and peak currents, which in turn minimizes conduction and turn-off losses and lowers capacitor stress. This also allows for the use of smaller filter components.

However, CCM operation comes with its own challenges. The continuous energy flow requires a larger transformer inductance, which often translates into a bulkier magnetic component. Additionally, the presence of a right half plane zero in the power stage transfer function limits the achievable bandwidth of the control loop, negatively affecting dynamic response. Moreover, controllers designed for valley switching are incompatible with CCM, as the transformer never fully demagnetizes, eliminating resonant ringing. Despite these drawbacks, the lower current stress and improved efficiency make CCM an attractive choice for high-power flyback designs.

A.2.1.2 DCM Mode of Operation

In DCM, the flyback converter is operated such that the transformer is fully demagnetized during each switching cycle. This is achieved by designing the power stage to allow the secondary winding current to decay completely to zero before the next cycle begins. A typical DCM flyback operates with a fixed switching frequency while modulating the peak primary current in response to the load demand.

At the beginning of each switching cycle, the power switch (typically a MOSFET) is turned ON, and the primary current linearly ramps up from zero, resulting in energy being stored in the transformer's magnetizing inductance. When the switch is turned OFF at the end of the on-time, the energy stored in the core is transferred to the secondary through the diode. The secondary current starts at a peak value determined by the turns ratio and then ramps down to zero, completely discharging the magnetic energy [92].

Following this demagnetization, there exists a time interval known as dead time or resonant time, during which neither the switch nor the diode conducts. This period is characterized by zero current conduction on both the primary and secondary sides, which is the defining feature of the discontinuous mode. The presence of this non conducting

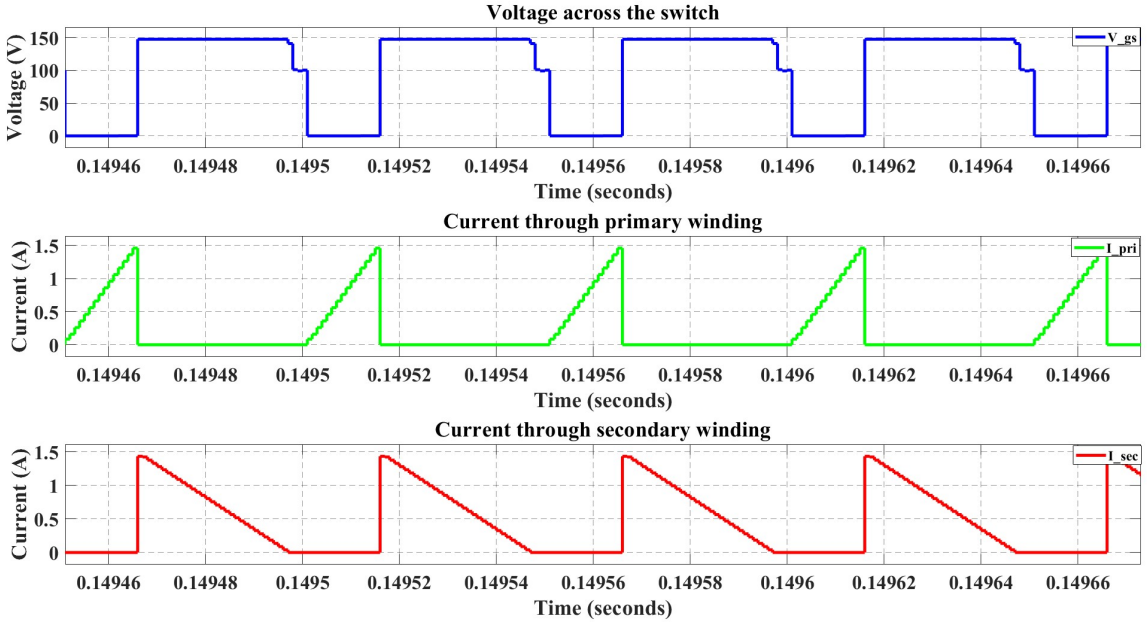


FIGURE A.2.5: Waveform for DCM Mode of Operation

interval gives DCM its name. Figure A.2.5 represents the output of flyback converter in DCM mode of operation.

During this dead time, a high frequency resonant ringing occurs due to the interaction between the leakage inductance of the transformer and the parasitic capacitance at the switching node. In deeply discontinuous operation, this ringing may fully decay, allowing the switch node voltage to settle close to the input supply voltage. This natural resonance can be exploited in valley switching techniques to minimize switching losses.

DCM operation is particularly advantageous in low load conditions, enabling simpler control schemes and reduced electromagnetic interference (EMI). However, it typically results in higher peak currents and increased core losses compared to continuous conduction mode (CCM).

A.2.1.3 Valley Switching Mode

Valley switching is an advanced switching strategy applied to flyback converters operating in Discontinuous Conduction Mode (DCM). In DCM, the power stage is designed such that the transformer's magnetizing current fully discharges during each switching cycle.

This ensures that the core is completely demagnetized before the next conduction period begins.

The operation begins when the primary switch (typically a MOSFET) turns ON, causing the primary current to ramp up from zero and store energy in the transformer's magnetizing inductance. At the end of the ON period, the switch is turned OFF, and the energy stored in the transformer is transferred to the secondary side. The resulting secondary current—proportional to the primary current and transformer turns ratio—ramps down to zero, thereby fully demagnetizing the core during each switching cycle.

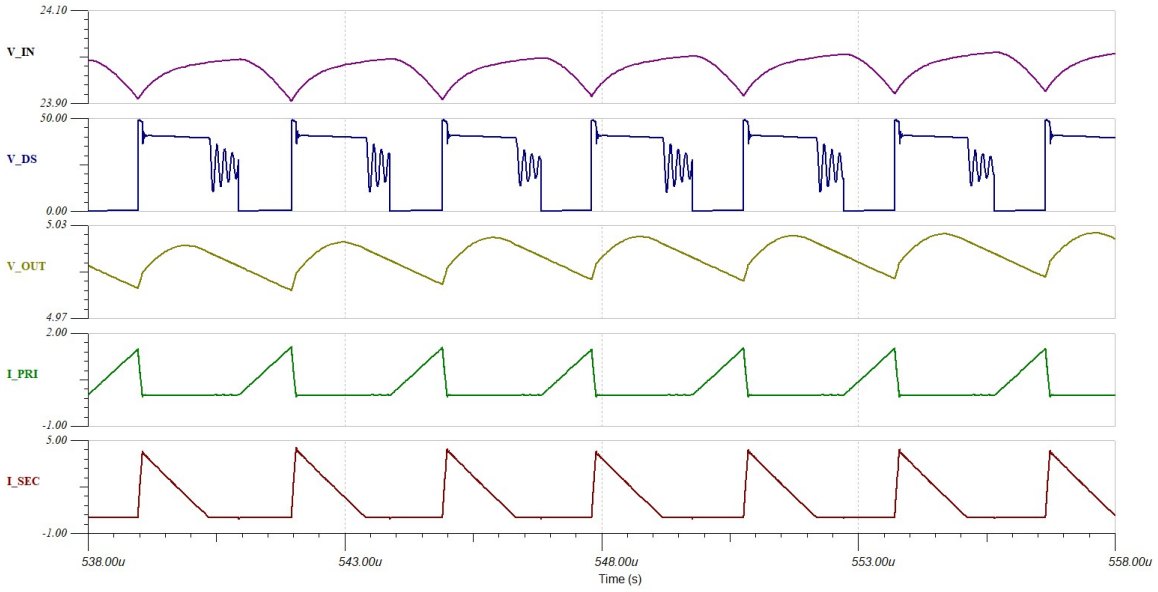


FIGURE A.2.6: Waveform for Valley Switching Mode

Following the demagnetization phase, a dead-time or resonant interval occurs. During this period, neither the primary switch nor the secondary diode conducts. Instead, a high-frequency ringing occurs at the switching node, caused by the resonance between the transformer's leakage inductance and the parasitic capacitance at the drain of the MOSFET. This resonant behavior creates voltage valleys at the MOSFET drain, which can be exploited to improve switching performance [93].

Figure A.2.6 represents the output of flyback converter in valley switching mode. In valley switching operation, the controller monitors the oscillating drain-to-source voltage

and initiates the next switching cycle precisely at the voltage minimum (i.e., the valley). By turning the MOSFET ON at this low-voltage point, switching losses are significantly reduced, as the device encounters lower drain to source voltage and reduced current overlap. This also mitigates the current spike at the sense resistor during turn-on, leading to improved efficiency and thermal performance.

Moreover, the slight frequency variation caused by valley skipping introduces natural frequency dithering, which contributes to reduced electromagnetic interference (EMI). However, valley switching is not without limitations. In deep DCM, where the dead-time is long and the oscillation amplitude diminishes, the controller may fail to detect a distinct valley. In such cases, valley switching becomes ineffective, and conventional fixed-frequency operation must be restored. Additionally, valley skipping can increase output voltage ripple due to the variable switching frequency.

Despite these constraints, valley switching offers a favorable compromise between the simplicity of DCM and the efficiency of soft-switching techniques, making it highly suitable for modern flyback-based USB Power Delivery (USB-PD) applications.

A.2.1.4 Quasi Resonant Mode of Operation

Quasi-Resonant (QR) mode is a high efficiency switching technique applied to flyback converters, particularly suitable for applications below 250W. Unlike conventional fixed frequency flyback designs that suffer from hard switching losses and high voltage stress on the MOSFET, QR mode leverages soft switching by initiating each switching cycle at the lowest point (valley) of the drain source voltage oscillation [94, 95].

QR operation is essentially a valley-switching variant of Discontinuous Conduction Mode (DCM), in which the switch is turned on at the first resonant valley after the transformer fully demagnetizes. This minimizes the voltage across the MOSFET during turn-on, significantly reducing switching losses and enhancing converter efficiency. Moreover, soft switching in QR mode leads to reduced electromagnetic interference (EMI), allowing for smaller EMI filters.

The QR flyback converter operates through three distinct modes in each switching cycle:

- **Mode 1: Switch ON (Energy Storage Phase)**

  The primary switch S turns ON, reverse-biasing the output diode D. The input voltage charges the magnetizing inductance L_m, and the primary current i_{Lm} increases linearly. The load is powered by the output capacitor C_o during this interval.

- **Mode 2: Switch OFF (Energy Transfer Phase)**

  When the switch turns OFF, the energy stored in L_m is transferred to the output through the now-forward-biased diode D. The reflected output voltage appears across the primary winding, and the secondary current ramps down until the transformer is fully demagnetized.

- **Mode 3: Resonant Interval (Valley Detection Phase)**

  After demagnetization, both the switch and diode remain OFF. The leakage inductance and MOSFET output capacitance C_{DS} form a resonant tank, causing the drain-source voltage to oscillate. Once the lowest valley is detected, the switch is turned ON to begin the next cycle.

QR controllers dynamically modulate both the *switching frequency* and the *peak current* to optimize efficiency across varying load conditions. At light loads, the frequency increases to reduce current stress, whereas at heavy loads, the frequency decreases to avoid excessive conduction losses. This combined amplitude and frequency modulation enables high performance over a wide operating range.

However, QR converters also present certain control and stability challenges. Their wide variation in switching frequency and peak current complicates compensation design and demands a substantial phase margin to ensure stability. Additionally, the QR condition turning ON precisely at the first resonant valley is only maintained reliably under specific

conditions (typically minimum input voltage and maximum load), unless a dedicated QR controller is used. Figure A.2.7 represents the output of flyback converter in QR mode.

Despite these complexities, QR flyback converters are widely favored for their excellent trade-off between efficiency, cost, EMI performance, and suitability for compact power supplies. Though standard valley-switching controllers can also operate in QR mode under well-defined conditions.

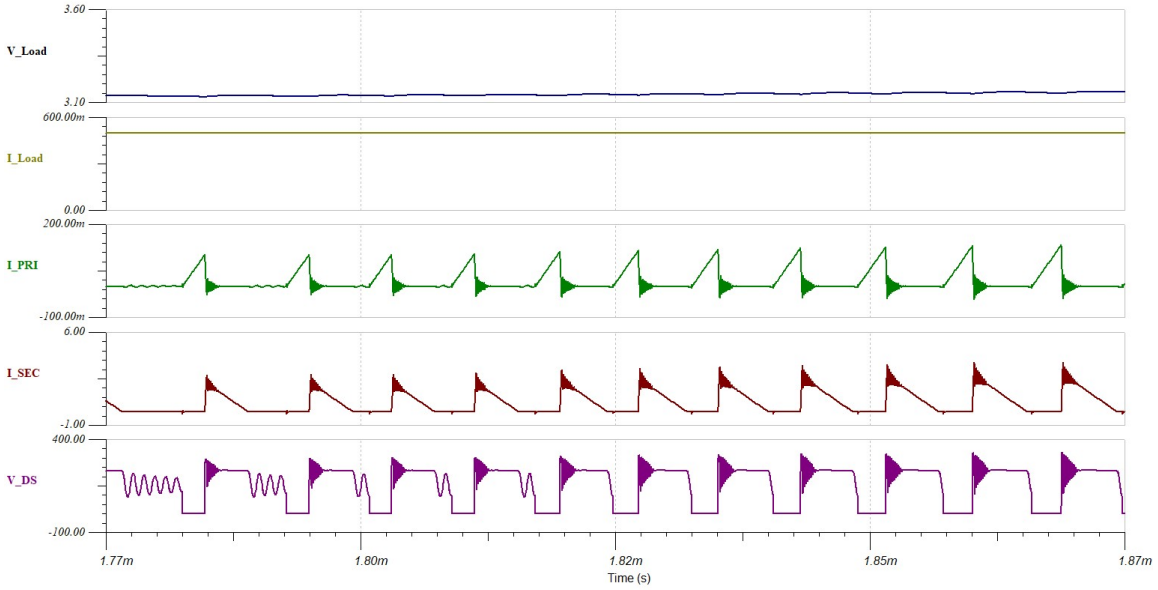


FIGURE A.2.7: Quasi-Resonant Converter Mode of Operation

Having established the fundamental operation and advantages of flyback converters—particularly in Quasi-Resonant (QR) mode—the discussion now transitions toward their practical application within standardized charging solutions. One of the most prominent advancements in this domain is the USB Power Delivery (USB-PD) specification, which offers a unified, scalable framework for power negotiation and delivery across a broad spectrum of electronic devices. The subsequent chapter provides an in-depth analysis of USB-PD technology, detailing its protocol architecture, power profiles, and the integration challenges addressed by flyback-based converter designs in modern charger applications.

A.2.2 Conclusion

This chapter presented a detailed analysis of the fundamental operation of Flyback Converters, emphasizing their versatility and efficiency in power conversion, particularly under Quasi-Resonant (QR) mode. The examination of switching dynamics, energy storage, and transfer mechanisms provided a clear understanding of how Flyback Converters achieve isolated power transfer while maintaining high efficiency across varying load conditions.

The insights gained from this chapter underscore the Flyback topology's suitability for low to medium power applications, such as USB PD chargers, auxiliary power supplies, and portable electronic adapters. Its ability to handle wide input voltage ranges with minimal complexity makes it an ideal candidate for integration into modern power delivery systems.

With a strong foundation established, the subsequent chapter transitions into the application of Flyback Converters within the USB Power Delivery (USB-PD) specification.

USB PD TECHNOLOGY

A.3.1 Introduction

With the proliferation of portable electronic devices such as smartphones, tablets, and laptops, the demand for compact, high-efficiency power adapters has surged. Traditionally, each device required a dedicated adapter, leading to a significant accumulation of redundant electronic waste. In response to growing environmental concerns and the need for user convenience, efforts have been made to standardize charging interfaces.

In 2014, the Universal Serial Bus Implementers Forum (USB-IF) introduced USB Type-C version 1.0. This new connector standard provided multiple advantages: a smaller reversible design, support for bidirectional power and data transmission, compatibility with audio and video interfaces, faster data rates, and enhanced power delivery capabilities of up to 20V/5A. To further unify charging solutions, the USB Power Delivery (PD) specification was updated in 2017 to include the Programmable Power Supply (PPS) feature under USB PD 3.0. This feature allows intelligent communication between the power source and the load to dynamically adjust the voltage and current based on real-time demands. The latest USB PD 3.1 update extends power delivery capability up to 28V/5A [96].

A.3.2 USB-PD Charger Specifications and Challenges

USB PD has become the industry standard for a wide range of digital devices including smartphones, tablets, laptops, and monitors. USB-PD chargers utilize the USB Type-C interface, simplifying the user experience and reducing the number of unique charging solutions. As shown in Table A.3.1, USB PD is classified into five profiles, with Profile 1

delivering up to 15W, suitable for handheld devices, and Profile 5 delivering up to 100W, suitable for larger equipment like LCD monitors.

For Profile 5 applications, the converter must handle a wide input voltage range (typically 100–240V AC) and provide output voltages in the range of 5–20V, posing efficiency challenges. Maintaining high efficiency across this wide operating window requires careful design choices, particularly in the power conversion topology.

TABLE A.3.1: USB Power Delivery (USB-PD) Profiles

Profile	Voltage (V)	Current (A)	Max Power (W)
1	5	3.0	15
2	5, 12	3.0	36
3	5, 12, 20	3.0	60
4	5, 12, 20	5.0	100
5	5–20 (PPS)	5.0	100

A.3.3 Flyback Converter in USB-PD Chargers

Among various topologies, the flyback converter is widely adopted for low to medium power applications due to its simplicity, cost-effectiveness, and ability to handle wide input-output voltage variations. The growth in fast charging standards and miniaturization trends has intensified the need for high power density and thermal efficiency in USB-PD adapters.

To achieve these performance goals, enhancements in the flyback topology are being pursued. For instance, Zero Voltage Switching (ZVS) techniques are employed to reduce switching losses and enable higher frequency operation, which in turn allows for smaller magnetic components. Primary-side controlled flyback converters with auxiliary windings and ZVS switches have been proposed, although they introduce challenges such as false triggering of synchronous rectifier (SR) MOSFETs and increased system complexity. Alternatives like Active Clamp Flyback (ACF) topology recover leakage energy and enable ZVS but require additional high-side switches and drivers, raising implementation costs.

A.3.4 System Level Design Considerations

Modern USB-PD 3.1 chargers are expected to support 90–264V AC input and programmable output voltages ranging from 5V to 21V, with fine 20mV steps. This mandates tight voltage regulation, high efficiency, and compact size. Flyback converters continue to be the preferred choice for such applications owing to their ability to balance these design trade-offs.

Recent advancements, such as the integration of Gallium Nitride (GaN) power devices, have further pushed the limits of performance, enhancing power density and efficiency. However, USB-PD functionality, SR control, and PWM regulation still necessitate the use of dedicated controller ICs.

Despite improvements in SR performance through primary-side control techniques, the necessity for independent SR controllers and opto-couplers as isolation elements introduces reliability concerns and design complexity. Opto-couplers, for instance, are known to degrade over time, compromising long-term system performance.

The USB-PD standard has streamlined the charging ecosystem by unifying multiple voltage and current profiles into a single interface. Flyback converters, due to their flexible design and cost advantages, remain central to USB-PD power supply development. However, future improvements must address the limitations in synchronous rectification, isolation techniques, and overall integration to meet evolving efficiency, size, and cost targets. Continued innovation in controller architecture and topological refinement is key to sustaining the next generation of USB-PD power delivery systems.

Figure A.3.1 represents the pinout for teh USB type C interface. USB Power Delivery (USB PD) has significantly evolved the role of USB from a basic data transfer interface to a comprehensive and intelligent standard for both power and communication. Initially developed to connect peripherals, USB is now widely adopted as a primary power source for various electronic devices, including smartphones, tablets, laptops, external drives,

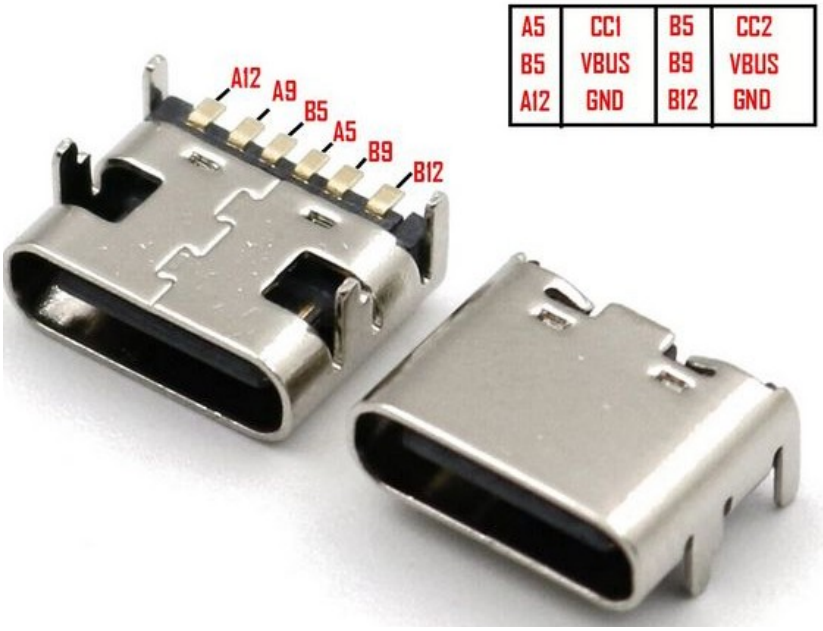


FIGURE A.3.1: Pinout for USB Type C

monitors, and even high-power applications such as e-scooters. This shift is driven by the growing need for higher power levels delivered efficiently and safely.

USB PD enables dynamic power negotiation between the source (e.g., charger) and the sink (e.g., device) over the USB Type-C interface. Unlike earlier USB standards limited to low power levels, USB PD supports delivery of up to 100W (20V, 5 A), achieved through intelligent voltage and current negotiation mechanisms. This not only reduces power losses by minimizing current levels at higher voltages but also alleviates thermal stress on components.

Communication between devices occurs over the configuration channel (CC) lines using Biphase Mark Code (BMC) signaling. This ensures accurate data transmission with minimal interference. Initially, USB PD protocols used Frequency-Shift Keying (FSK) over the VBUS line, but this was later replaced by BMC on the CC lines for improved simplicity and reliability [97].

The communication sequence begins with connection detection: the power source applies a pull-up resistor to the CC line, while the sink applies a pull-down resistor, thereby establishing a reference voltage to confirm connectivity. Once detected, the

source advertises its supported power profiles, and the sink selects the most suitable one based on its power requirements. The power contract is finalized, and delivery begins only after successful negotiation, ensuring both safety and efficiency.

USB Type-C connectors further enhance this protocol with their reversible design, eliminating orientation issues, and supporting multiple high-speed protocols including USB 3.1, DisplayPort, HDMI, Thunderbolt, and USB4. Advanced USB PD features include role swapping, allowing devices to function alternately as power sources or sinks, and structured vendor-defined messages (VDMs) for extended communication. Built-in safety mechanisms—such as voltage and current monitoring—further ensure protection during high-power transfers.

To protect against electrostatic discharge (ESD) and voltage spikes, especially on the CC1 and CC2 pins responsible for communication and role detection, integrated surge protectors and termination resistors are employed. These measures safeguard sensitive low-voltage components and ensure long-term system reliability.

With its robust protocol structure, scalable power profiles, and versatile data integration, USB PD has become a cornerstone of modern electronics. Its ability to deliver tailored power while maintaining safety and communication integrity makes it a highly adaptable and future-proof charging solution.

A.3.5 Conclusion

With a comprehensive understanding of the USB Power Delivery protocol and its operational requirements, the focus now shifts to the design of the flyback converter topology, which serves as a critical building block in implementing compact, efficient, and programmable USB PD charger systems.

FLYBACK CONVERTER DESIGN

A.4.1 Introduction

The flyback converter is a widely utilized topology in isolated power supply applications due to its simplicity, cost-effectiveness, and ability to handle multiple output voltages. It operates on the principle of energy storage in a magnetic field during the switch-on period, which is then transferred to the load during the switch-off period. This design process details the complete calculations for transformer design, voltage stress estimation, and current determination to ensure optimal converter performance.

A.4.2 Design Equations

Table A.4.1 outlines the key specifications considered for the converter design. These parameters serve as the foundation for all subsequent design calculations.

TABLE A.4.1: Key Design Parameters

Parameter	**Value**
Input Voltage Range (V_{in})	90V – 265V (Universal)
Minimum Input Voltage (V_{in_min})	90 VAC
Maximum Output Voltage (V_{out_max})	20 V
Maximum Output Current (I_{out_max})	3 A
Maximum Duty Cycle (D_{max})	0.627

A.4.2.1 Turns Ratio Calculation

The turns ratio of the flyback transformer is determined using the minimum input voltage, the desired output voltage, and the maximum duty cycle:

$$\frac{N_p}{N_s} = \frac{V_{\text{in(min)}}}{V_{\text{out}} + V_d} \times \frac{D_{\max}}{1 - D_{\max}} \tag{17}$$

Substituting the values:

$$\frac{N_p}{N_s} = \frac{90}{21 + 0.7} \times \frac{0.627}{1 - 0.627} \tag{18}$$

$$\frac{N_p}{N_s} = n = 7 \tag{19}$$

A.4.2.2 Voltage Stress on the Switch

The maximum voltage stress experienced by the MOSFET switch is calculated as follows:

$$V_{\text{ds\_max}} = V_{\text{in\_max}} + n \cdot (V_{\text{out}} + V_d) \tag{20}$$

$$V_{\text{ds\_max}} = 265 + 7 \times (21 + 0.7) = 413.9\,\text{V} \tag{21}$$

A.4.2.3 Minimum Inductance Calculation

The minimum primary inductance is determined to ensure proper energy storage during the switching cycle [91]:

$$L_{\text{min\_pri}} = \frac{V_{\text{in\_min}}^2 \times d_{\text{max}}^2 \times \eta}{2 \times f_{\text{sw}} \times P_{\text{out\_min}}} \tag{22}$$

$$L_{\text{min\_pri}} = \frac{90^2 \times (0.627)^2 \times 0.91}{2 \times 71070 \times 60} \tag{23}$$

$$L_{\text{min\_pri}} = 469.17\,\mu\text{H} \tag{24}$$

The secondary side inductance is derived as:

$$L_{\text{min\_sec}} = \frac{L_{\text{min\_pri}}}{n^2} = \frac{469.17}{7^2} \tag{25}$$

$$L_{\text{min\_sec}} = 9.245\,\mu\text{H} \tag{26}$$

A.4.2.4 Primary and Secondary Current Calculations

The peak primary current is given by:

$$I_{\text{pri\_pk}} = \frac{I_{\text{out\_max}}}{(1 - d_{\text{max}}) \cdot n} + \frac{V_{\text{in\_min}} \times d_{\text{max}}}{2 \times L_{\text{min\_pri}} \times f_{\text{sw}}} \tag{27}$$

$$I_{\text{pri\_pk}} = \frac{3}{(1 - 0.627) \cdot 7} + \frac{90 \cdot 0.627}{2 \cdot 469.17 \cdot 71070} \tag{28}$$

$$I_{\text{pri\_pk}} = 1.149\,\text{A} \tag{29}$$

The secondary peak current is calculated as:

$$I_{\text{sec\_pk}} = I_{\text{pri\_pk}} \cdot n = 1.149 \cdot 7 \tag{30}$$

$$I_{\text{sec\_pk}} = 8.043\,\text{A} \tag{31}$$

A.4.2.5 Core Flux Density Calculation

The flux density variation is derived as:

$$\Delta B_{\max} = B_{\max} \cdot \frac{\Delta I_{\text{sec\_pk}}}{I_{sc}} \tag{32}$$

$$\Delta B_{\max} = 0.04\,\text{T} \tag{33}$$

The tentative core type selected is EQ core with following specifications: Effective core area: A_e = 100 mm^2 Volume: V_e = 4145 mm^3 Path length: l_e = 41.4 mm Center pole parameter: DCP = 11.12 mm

The secondary number of turns can be calculated as:

$$N_s = \frac{L_{\text{sec}} \cdot \Delta I_{\max}}{\Delta B_{\max} \cdot A_e} \cdot 10^{-2} \tag{34}$$

$$N_s = \frac{9.245 \cdot 14.264}{0.04 \cdot 0.95} \cdot 10^{-2} \tag{35}$$

$$N_s = 4.74 \approx 5 \text{ turns} \tag{36}$$

$$N_p = 5 \cdot 7 = 35 \text{ turns} \tag{37}$$

Thus, the complete transformer design is finalized, and the subsequent section presents the electrical winding diagram in detail.

A.4.2.6 Winding Diagram for Transformer

Figure A.4.1 presents the electrical winding diagram based on the calculated specifications. The required voltages for the secondary and bias windings are appropriately adjusted, and the Average Wire Gauge (AWG) is selected according to the

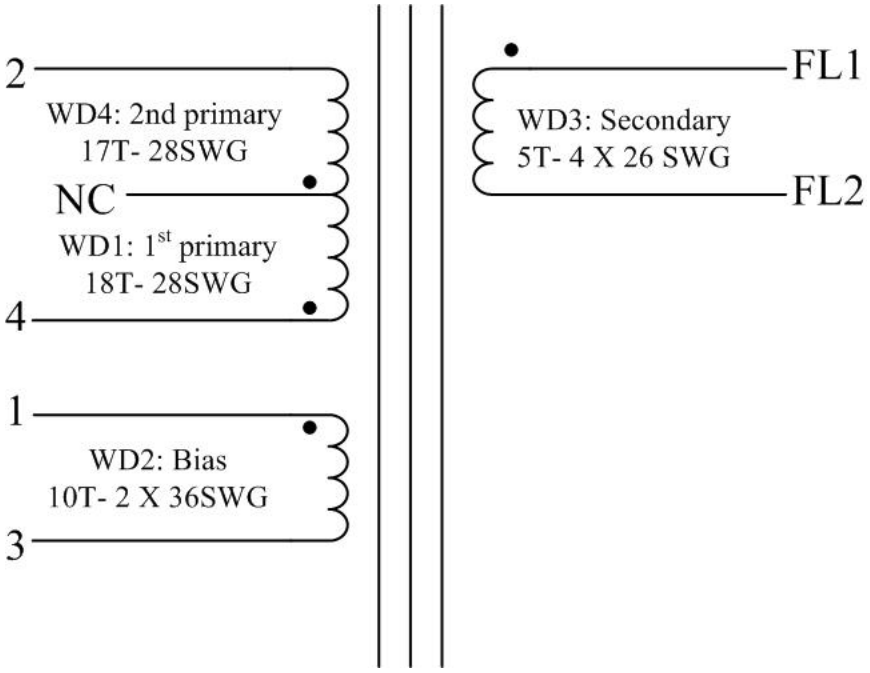


FIGURE A.4.1: Electrical Diagram for Transformer

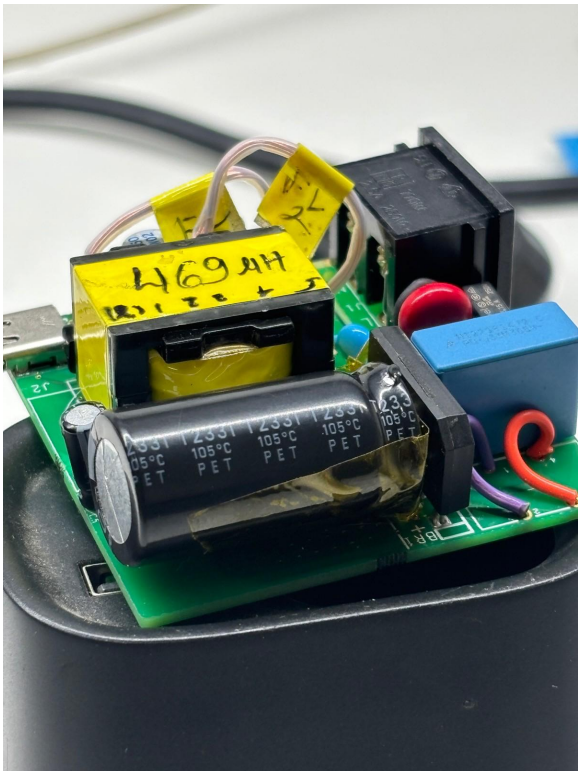


FIGURE A.4.2: Actual Photograph of Transformer

current requirements. Additionally, a bobbin was designed and 3D printed to accommodate these adjustments.

Figure A.4.2 displays the actual photograph of the transformer mounted on the PCB, featuring the 3D printed bobbin. The bobbin design was developed using Autodesk Fusion software and subsequently 3D printed to match the core's dimensions.

A.4.3 Power Stage Design

The power stage of the Flyback Converter is a critical component responsible for voltage conversion and isolation. Figure A.4.3 illustrates the complete schematic of the power stage, showcasing its essential elements including the input rectification, snubber circuit, switching mechanism, and transformer configuration.

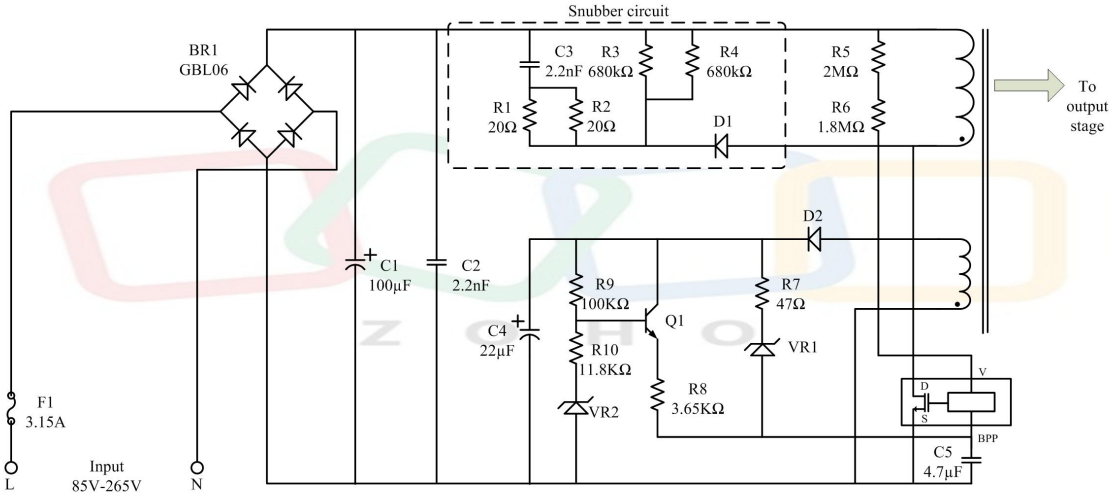


FIGURE A.4.3: Power Stage of Flyback Converter

The input AC voltage, ranging from 85V to 265V, is fed through a fuse (F1) rated at 3.15A for overcurrent protection. The AC voltage is then rectified using a bridge rectifier (BR1, GBL06), converting it to DC. The rectified voltage is filtered by the bulk capacitor C1 (100μF), which smoothens the DC signal before feeding it to the primary side of the transformer.

The Flyback transformer serves as both an energy storage element and an isolation barrier between the primary and secondary sides. During the switching cycle, energy is stored in the magnetic field of the transformer when the primary switch (Q1) is turned on. This switch is controlled through a feedback mechanism that regulates the output voltage. The energy stored in the magnetic field is transferred to the secondary side during the off-period of the switch.

To protect against voltage spikes generated by transformer leakage inductance, a snubber circuit is employed. The snubber circuit, consisting of resistors (R1, R2, R3, R4), capacitor (C3), and diode (D1), effectively suppresses transients, thereby protecting the switching device from damage and minimizing electromagnetic interference (EMI).

On the secondary side, the energy transferred through the transformer is rectified by diode D2 and filtered by the capacitive elements, ensuring a stable DC output. Additionally, the gate drive circuitry, represented by components R9, R10, VR1, and VR2, manages the switching operations of Q1, ensuring precise control over the energy transfer process.

The power stage is designed to handle wide input voltage ranges efficiently while maintaining isolation and delivering regulated output to the subsequent output stage. This stage is critical in applications such as USB PD chargers and auxiliary power supplies, where efficiency, reliability, and voltage stability are paramount.

The output stage of the Flyback Converter is engineered to provide stable voltage and current to the load while ensuring efficiency and robust protection. Figure A.4.4 illustrates the complete schematic of the output stage, highlighting critical components such as synchronous rectification, voltage and current sensing, USB PD communication, and protection circuitry.

On the secondary side, the IC handles voltage and current sensing, along with the gate drive for the synchronous rectification (SR) FET Q2. The transformer's secondary winding generates a voltage that is rectified by Q2 and filtered using capacitors C12 and C13 to deliver a smooth DC output. To suppress high-frequency ringing during switching

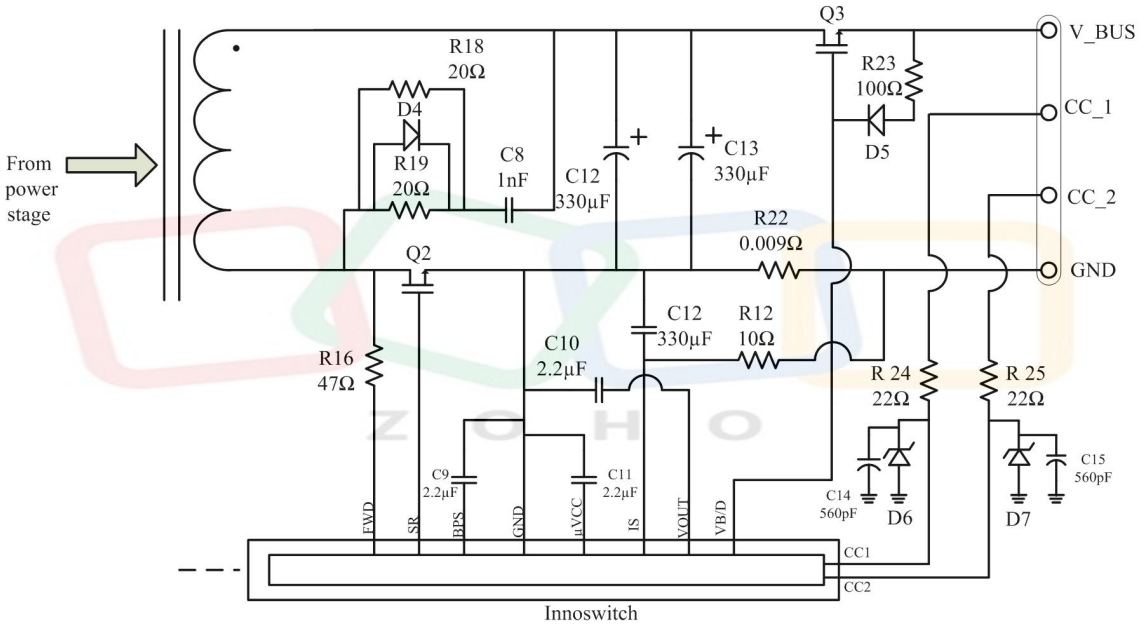


FIGURE A.4.4: Output Stage for Flyback Converter

transients, an RCD snubber network (R18, R19, C8, and D4) is included, effectively minimizing electromagnetic interference (EMI).

The gate of Q2 is regulated by the secondary controller within IC U1. Voltage from the secondary winding is sensed through resistor R16 and fed into the FWD pin of the IC. In continuous conduction mode (CCM), the SR FET is deactivated just before the secondary controller triggers a new switching cycle on the primary side. Conversely, in discontinuous conduction mode (DCM), the SR FET is turned off when the voltage drop across it falls below a preset threshold ($V_{SR(TH)}$). This precise secondary-side control eliminates the possibility of cross-conduction, ensuring reliable synchronous rectification.

The secondary side of IC U1 is self-powered either from the forward voltage of the secondary winding or directly from the output voltage. Capacitor C9, linked to the BPS pin of IC U1, provides the necessary decoupling for its internal circuitry.

Current sensing is achieved by measuring the voltage drop across resistor R22. This voltage is filtered using a decoupling network composed of capacitor C7 and resistor R12 and is monitored across the IS and Secondary Ground pins. An internal current sense threshold, configured via firmware, is set up to approximately 32 mV. When the sensed

voltage surpasses this threshold, IC U1 modulates the number of switching pulses to maintain a stable output current.

During Constant Current (CC) operation, if the output voltage decreases, the secondary controller within IC U1 draws power directly from the secondary winding. During the on-state of the primary switch, the forward voltage from the secondary winding recharges the Secondary Bypass pin decoupling capacitor (C9) through resistor R16 and an internal regulator. This enables the converter to regulate current down to its minimum undervoltage threshold. If the voltage drops below this limit, the converter enters auto-restart mode until the load is reduced.

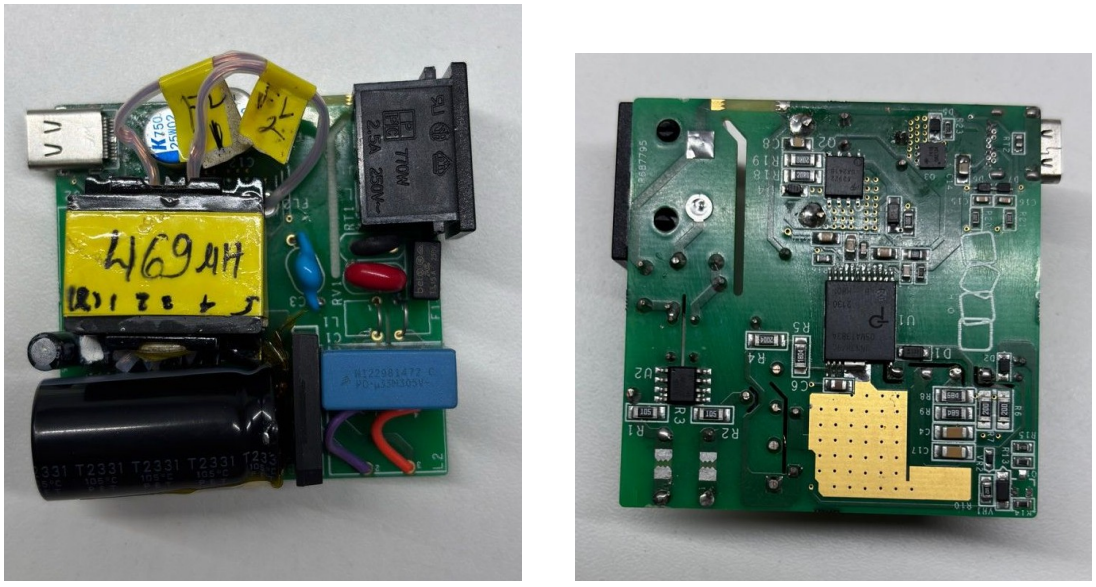
When the output current is below the CC limit, the converter operates in Constant Voltage (CV) mode. In this mode, the output voltage is monitored by the VOUT pin of IC U1, where it is compared to an internal reference. The internal controller adjusts the switching pulses to maintain voltage regulation. Capacitor C10 is placed between the VOUT pin and Secondary Ground to provide electrostatic discharge (ESD) protection.

An N-channel MOSFET (Q3) serves as the bus switch, managing the connection between the Flyback Converter's output and the USB Type-C receptacle. Q3 is driven by the VB/D pin on IC U1. Resistor R23 and diode D5 are connected across the Source and Gate terminals of Q3, ensuring a discharge path for bus voltage when Q3 is deactivated. Capacitor C14 is incorporated to protect the output from ESD events.

USB PD communication is facilitated over either CC1 or CC2, depending on the orientation of the Type-C connection. Capacitor C11 provides decoupling for the μVCC supply of IC U1. Additional protection for communication lines is achieved using capacitors C15 and C16, resistors R20 and R21, and Zener diodes D6 and D7, effectively shielding CC1 and CC2 from potential ESD damage.

This structured output stage not only guarantees efficient voltage and current regulation but also reinforces the reliability of the USB PD interface by mitigating transient voltage spikes and providing robust ESD protection.

A.4.4 PCB Layout of Flyback Converter



(A) Top View (B) Bottom View

FIGURE A.4.5: Actual Photograph of USB Type-C 60W Flyback Prototype for Biomedical Application

The PCB layout of the flyback converter is designed to optimize space and minimize parasitic inductances, which can cause losses and affect efficiency. The board is divided into key functional areas:

- **Primary Side:** This section includes the rectifier bridge, filter capacitors, and the MOSFET switch for primary energy storage.
- **Secondary Side:** The output rectification and filtering components are placed here, along with the feedback control circuitry.
- **Isolation and Snubber Region:** This area is dedicated to snubber components and isolation barriers to prevent noise from propagating through the power lines.

To implement the designed converter in hardware, a PCB was designed and fabricated. After the fabrication process, all components were mounted on the PCB. During the design of the PCB, careful consideration was given to reducing losses and ensuring efficiency.

Figure. A.4.5 shows the fabricated PCB with clearly marked primary and secondary stages. The layout is optimized for minimal loop inductance and efficient thermal management.

The PCB is designed to meet safety and electromagnetic compatibility (EMC) standards, ensuring reliable operation under various load conditions.

A.4.5 Conclusion

In summary, this chapter presented the detailed design methodology of a Flyback Converter integrated with a USB Power Delivery (USB PD) interface, intended to supply regulated power to an ECG monitor operating in multiple modes. The next chapter focuses on the hardware implementation of the proposed power supply, validating its performance through experimental testing under various load conditions.

RESULT AND DISCUSSION

A.5.1 Introduction

The design and implementation of the Flyback Converter provide a versatile solution for isolated power conversion in applications such as USB Power Delivery (USB PD) and auxiliary power supplies. However, evaluating its performance is critical to ensure reliability, efficiency, and optimal operation under varying load conditions. This chapter presents an in-depth analysis of the Flyback Converter's performance metrics, focusing on key parameters such as voltage ripple and efficiency.

Voltage ripple is an essential factor that influences the quality of power delivered to the load. In power electronics, minimizing voltage ripple is crucial for maintaining stable operation and preventing adverse effects on sensitive electronic components. The ripple magnitude is primarily influenced by factors such as switching frequency, filter capacitance, and transformer characteristics. This chapter investigates the voltage ripple behavior under different load conditions and analyzes the effectiveness of the implemented filtering techniques.

Furthermore, the efficiency of the Flyback Converter is a significant measure of its power conversion capability. It reflects the proportion of input power effectively transferred to the output, accounting for losses in the switching elements, magnetic components, and passive devices. Achieving high efficiency is critical for reducing thermal stress, enhancing power delivery, and meeting regulatory energy standards. Experimental results, including efficiency plots and thermal analysis, are presented to validate the converter's performance.

The subsequent sections provide a detailed breakdown of the testing methodology, measurement setups, and the analysis of the Flyback Converter's voltage ripple and efficiency across various load scenarios. The results obtained are benchmarked against industry standards to demonstrate the converter's capability in real-world applications.

A.5.2 Experimental Setup for USB PD Flyback Converter Testing

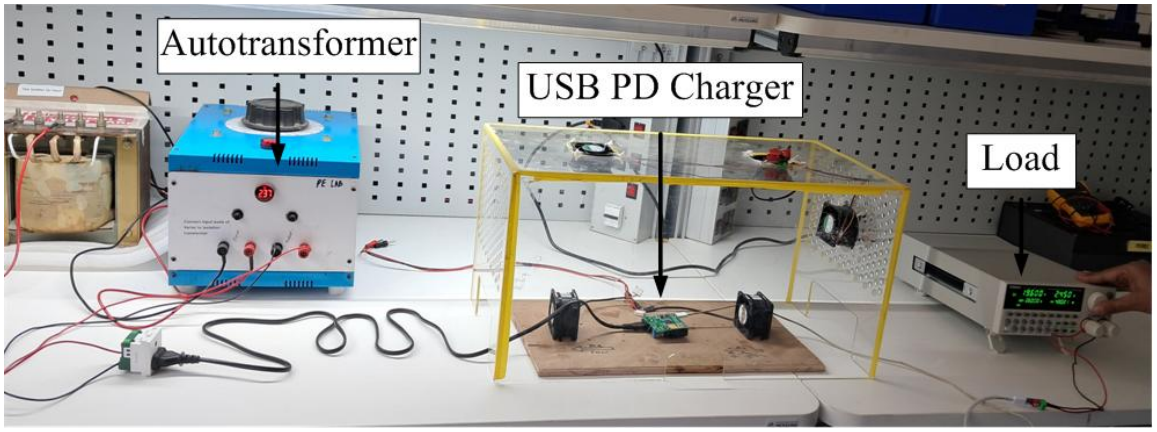


FIGURE A.5.1: Setup for Testing the Charger

Figure A.5.1 illustrates the experimental setup employed for testing the USB PD Flyback Converter. The charger is evaluated across a universal input voltage range of 90V to 265V, which is configured using an autotransformer. This setup allows for precise adjustment of the input voltage, enabling the assessment of the converter's performance under various grid conditions.

To replicate real-world application scenarios, a programmable DC load is connected to the output of the USB PD charger. This load is configured to simulate the power consumption characteristics of an ECG machine, mirroring its operational requirements. The testing procedure encompasses a wide range of current levels, spanning from no-load conditions to the maximum rated current of 3A. This thorough evaluation ensures that the converter's voltage regulation, efficiency, and ripple performance are validated across its full operating range.

The subsequent sections present a detailed analysis of the results obtained during testing, highlighting key performance metrics and their implications for biomedical power supply applications.

A.5.2.1 Startup of Charger

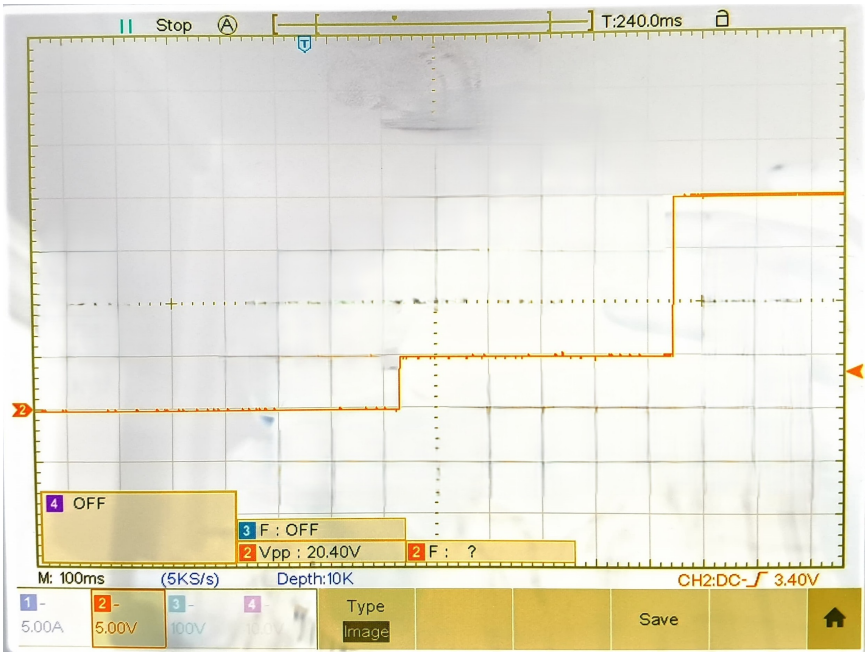
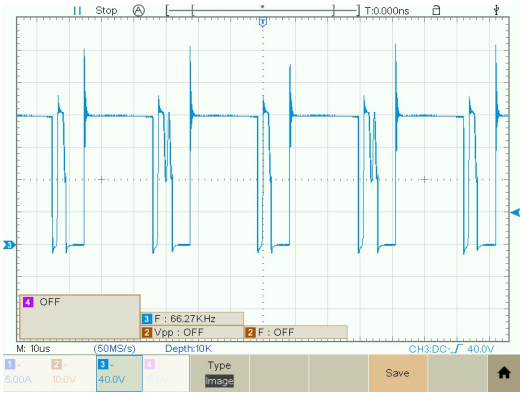


FIGURE A.5.2: Startup Waveform for USB PD Converter

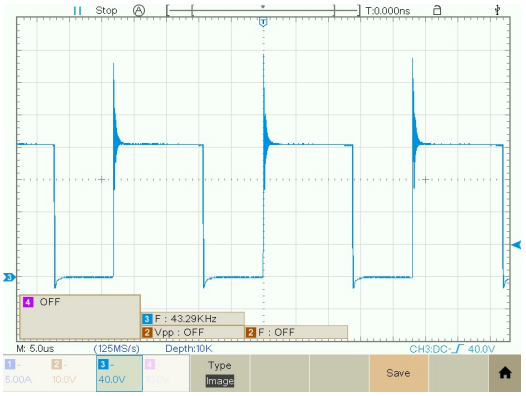
Figure A.5.2 illustrates the startup performance of the USB PD-based flyback charger when interfacing with the ECG monitor, which initially requests a 20V output. In accordance with the USB Power Delivery (USB PD) negotiation protocol, the charger first establishes communication with the load and begins by supplying a default voltage of 5V. This initial stage ensures proper device detection and safe voltage ramp-up. Once communication is successfully completed and the required voltage profile is confirmed, the charger transitions from 5V to the requested 20V output.

This startup waveform represents the dynamic voltage scaling behavior of the charger, showcasing its compliance with the USB PD specification. The smooth and controlled transition ensures reliable power delivery without imposing inrush stress on the ECG monitor or the charger's output stage. Such startup behavior is essential in medical applications, where consistent and stable voltage regulation is critical for device functionality and patient safety.

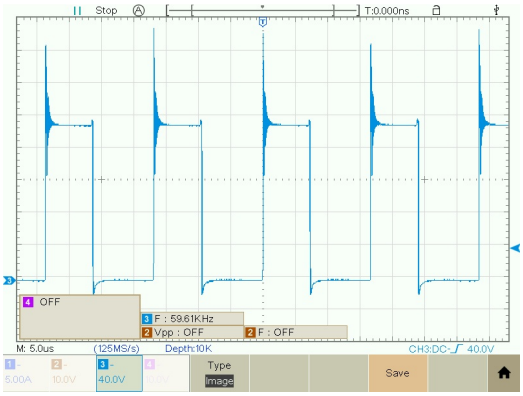
A.5.2.2 Performance of Converter at 90VAC



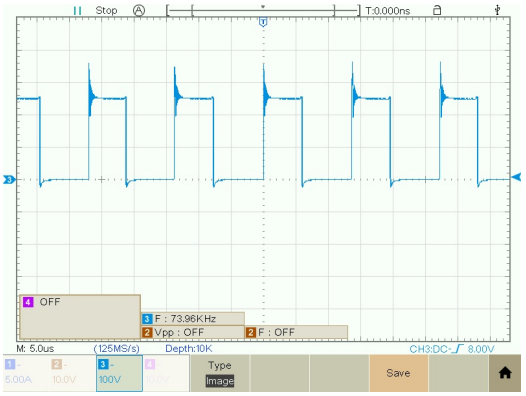
(A) At 5V Output



(B) At 9V Output



(C) At 15V Output



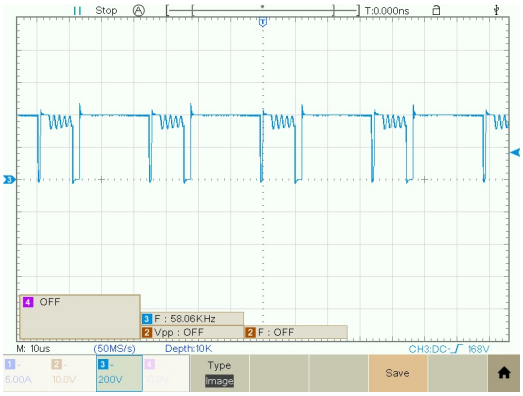
(D) At 20V Output

FIGURE A.5.3: Waveform for Voltage Across Drain to Source at 90V AC rms

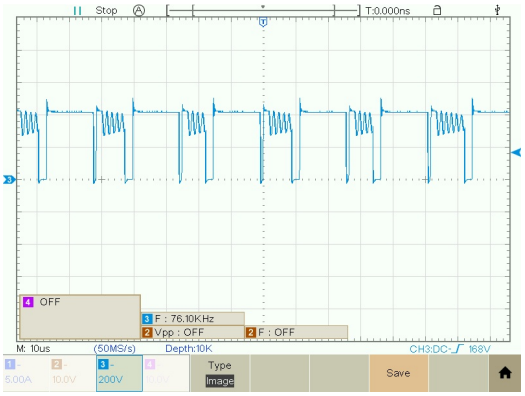
Figure A.5.3 illustrates the switching characteristics of the MOSFET when the input voltage is reduced to 90V. Under these conditions, the peak drain-to-source voltage is lower, and the ringing effects are diminished due to reduced energy storage in the transformer and decreased stress on the MOSFET.

Furthermore, the variations in frequency and duty cycle demonstrate how the converter dynamically adjusts its operation to maintain stable output power across different voltage levels. These observations indicate that the USB PD charger effectively regulates the output voltage while adapting to input fluctuations, thereby ensuring efficient performance across a wide operating range.

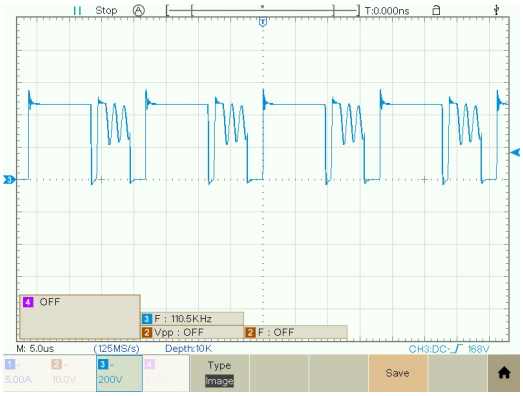
A.5.2.3 Performance of Converter at 265VAC



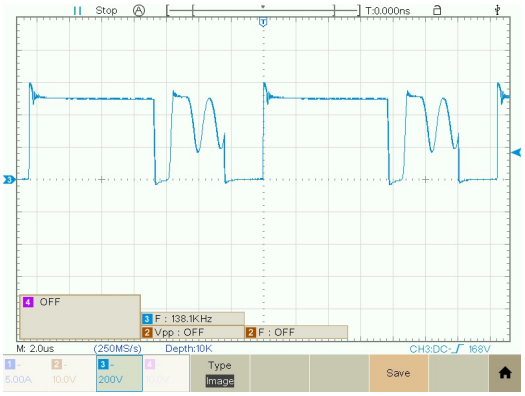
(A) At 5V Output



(B) At 9V Output



(C) At 15V Output



(D) At 20V Output

FIGURE A.5.4: Waveform for Voltage Across Drain to Source at 265V AC rms

Figure A.5.4 presents the drain-to-source voltage characteristics of a switching MOSFET within a power supply circuit, analyzed under various output voltage levels of 5V, 9V, 15V and 20V. The input is kept constant at the 265V AC rms. This figure is crucial for understanding the dynamic behavior of the MOSFET in different operational scenarios.

The variations in amplitude and switching behavior observed in the waveform reflect the MOSFET's performance under different load conditions and output voltages. Notably, at higher input voltages, the switching waveform shows more pronounced ringing and sharper transitions. This is mainly due to increased voltage stress and greater switching losses, which are characteristic of the MOSFET's operation at elevated voltage levels.

Additionally, the flyback converter operates in a valley switching mode, where it switches at the lowest valley point.

Moreover, as the output voltage level increases, there is a corresponding rise in the switching frequency of the converter. This increase in switching frequency is a critical parameter, as it affects the efficiency and thermal management of the power supply circuit. The relationship between input voltage, output voltage, and switching frequency highlights the complex interplay of factors that influence the MOSFET's switching characteristics.

A.5.2.4 Voltage Ripple at Worst Condition

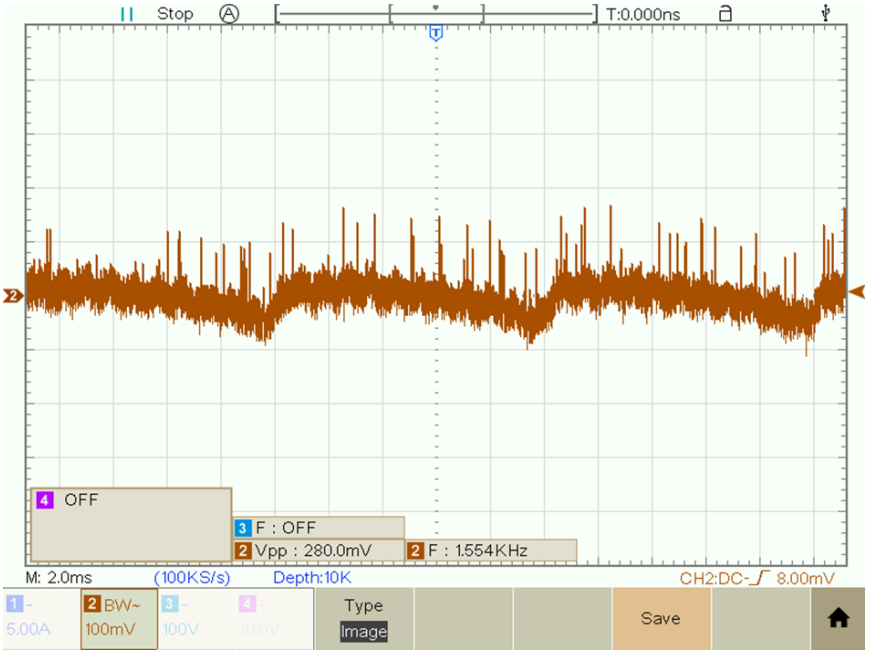


FIGURE A.5.5: Voltage Ripple at 90V AC rms Full Load

Figure A.5.5 depicts the voltage ripple at a full load condition with an input voltage of 90V, emphasizing the noise and fluctuations present in the output voltage. The observed ripple can be attributed to switching transients, parasitic elements, and load variations.

The presence of high-frequency components within the ripple waveform indicates the significant impact of switching characteristics. Despite these fluctuations, the voltage ripple remains within the acceptable limits set for biomedical applications, ensuring compliance with industry standards and reliable performance.

A.5.2.5 Efficiency of Converter

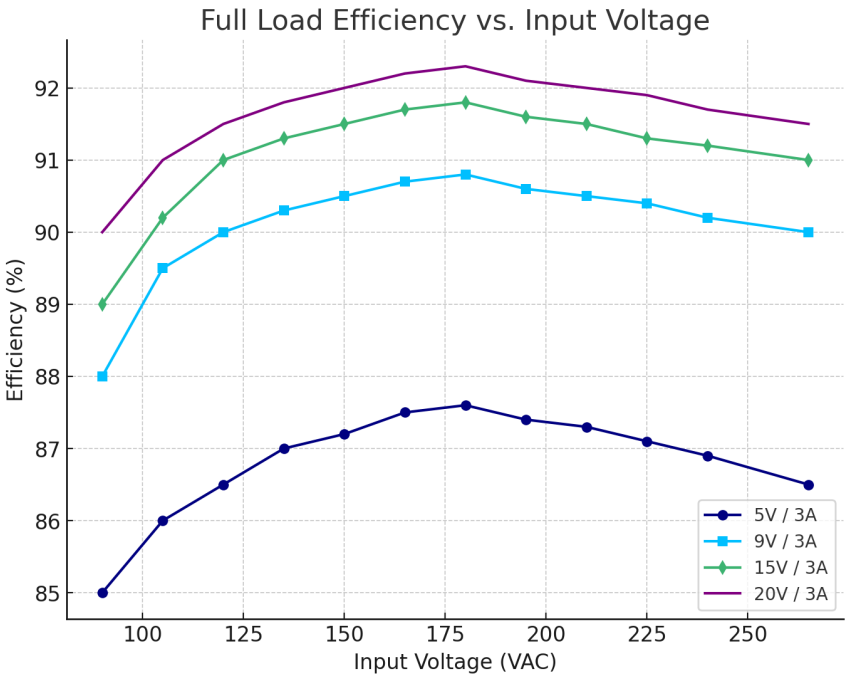


FIGURE A.5.6: Efficiency of the Converter in Different Modes

Figure A.5.6 illustrates the efficiency characteristics of the converter at full load across varying input voltages for different output levels. The efficiency trends reveal an optimal operating range, with peak efficiency observed in the 175V–200V AC range.

The variations in efficiency across different output voltages suggest that the USB PD charger effectively regulates power delivery while maintaining overall performance. Notably, the 5V output exhibits the lowest efficiency, primarily due to lower loading condition. This analysis underscores the converter's ability to adapt to varying input conditions while optimizing efficiency, which is crucial for ensuring reliable and efficient power delivery in diverse mode of operation of the ECG monitor.

A.5.2.6 Regulation of Converter

Figure A.5.7 illustrates the regulation performance of the USB PD charger. The results demonstrate stable regulation with minimal deviation, ensuring consistent output despite

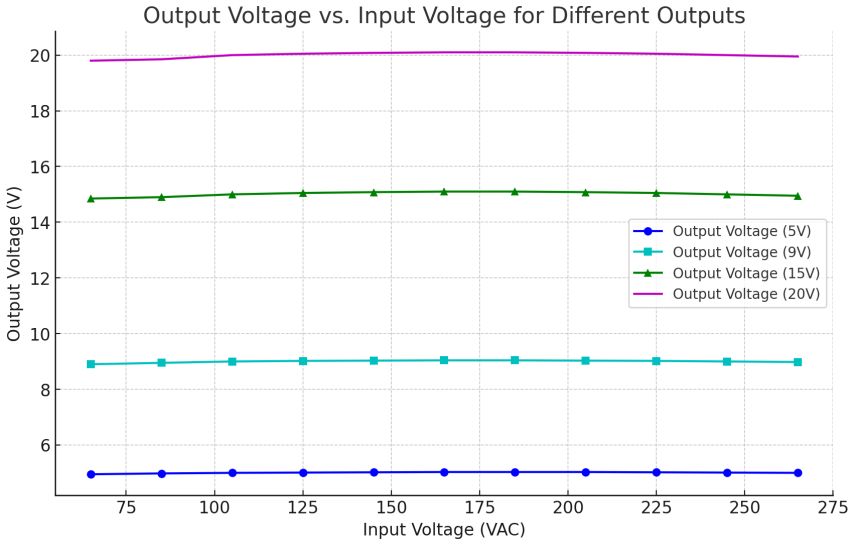


FIGURE A.5.7: Regulation of Converter for Different Modes

fluctuations in input voltage.

The 20V output maintains a nearly constant voltage profile, indicating the presence of a well-designed feedback mechanism. Overall, the regulation performance confirms the converter's capability to provide reliable voltage outputs under varying operating conditions, highlighting its robustness and efficiency in maintaining stable power delivery.

A.5.3 Conclusion

This chapter presented the hardware implementation and performance evaluation of the proposed Flyback Converter for USB PD charger applications. The converter was thoroughly tested under various operating conditions, and the results confirmed its suitability and reliability for real-world deployment. The USB PD charger demonstrated stable performance across a wide input voltage range and different load scenarios, validating the effectiveness of the design.

In addition, a dedicated DC load test was conducted to emulate the actual usage conditions. The results of these tests were consistent with expectations, showing excellent voltage regulation, low ripple, and efficient power conversion. In general, hardware

validation confirmed that the converter operates as intended, making it a strong candidate for integration into standardized USB PD charging solutions.

CONCLUSION AND FUTURE SCOPE

A.6.1 Conclusion

This thesis presents the design and development of a flyback converter with a USB Power Delivery (USB PD) interface, specifically tailored for biomedical applications. The primary objective was to develop a 60W USB PD flyback prototype and evaluate its performance under various conditions to ensure its suitability for biomedical devices.

The development process involved several stages, starting with the design phase, where the specifications and requirements for the flyback converter were meticulously defined. The design was then implemented, resulting in a prototype that was subjected to rigorous testing. These tests were conducted under different operating conditions to assess the converter's reliability, efficiency, and overall performance.

The results of these tests were promising, indicating that the flyback converter met the necessary criteria for biomedical applications. The converter demonstrated the capability to provide stable and precise power to an ECG monitor, which operates in multiple modes as specified in the problem statement. This successful implementation addresses the initial problem statement comprehensively.

In addition to its functional performance, the flyback converter features a universal input, making it versatile for use in various regions with different power standards. The precise power delivery is achieved through the USB PD protocol, ensuring that the connected biomedical devices receive the appropriate power levels required for their operation.

The hardware setup for the flyback converter was developed and tested in real-time scenarios, further validating its practical applicability. The successful real-time testing underscores the converter's readiness for deployment in biomedical settings.

In conclusion, this thesis has successfully addressed the problem statement by developing a flyback converter with a USB PD interface that meets the demands of biomedical applications. The converter's universal input capability and precise power delivery through the USB PD protocol are key features that enhance its utility and reliability. This work contributes to the advancement of power solutions for biomedical devices, ensuring they operate efficiently and safely.

A.6.2 Future Scope

The proposed work can be extended in multiple directions. One of the primary avenues for future enhancement involves increasing the power rating of the converter to accommodate higher load requirements and support more demanding biomedical applications. Additionally, the system may be augmented with multiple output rails capable of negotiating power contracts through the USB PD protocol. This multi rail configuration would enable simultaneous and efficient power distribution to various medical instruments connected to the system, thereby enhancing its versatility and utility in real-world clinical environments.

ANNEXURE B

MODELING OF ADVANCE GATE DRIVER FOR TRACTION INVERTER APPLICATION

Introduction

B.1.1 Literature Survey

Gate drivers are specialized electronic circuits designed to control and drive the gate of power semiconductor devices such as MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) and IGBTs (Insulated Gate Bipolar Transistors). Gate drivers are crucial in power electronics for switching applications, where they act as the interface between low-power control signals and high-power switching devices. Typically, gate drivers are designed based on worst-case scenarios to limit the switching di/dt and dv/dt, thereby preventing excessive surge voltage but increasing switching losses [98, 99].

B.1.1.1 What Gate Drivers Do

Gate drivers perform several essential functions:

- **Voltage Level Translation**: They convert low-voltage control signals from microcontrollers or digital signal processors into higher voltages required to operate power transistors.
- **Supply Current**: They provide the necessary current to charge and discharge the gate capacitance of power devices, ensuring swift and efficient switching.

- **Isolation**: In many applications, gate drivers provide electrical isolation between the control side and the power side to protect sensitive control circuitry from high voltages and currents.

B.1.1.2 Why Gate Drivers are Needed

Gate drivers are needed for several reasons:

- **Efficient Switching**: Power devices like MOSFETs and IGBTs have gate capacitances that need to be charged and discharged quickly to achieve efficient switching. Gate drivers supply the required current to overcome this capacitance.
- **Protection**: Gate drivers often include protection features such as under-voltage lockout, over-current protection, and thermal shutdown to safeguard both the power device and the driver itself.
- **Performance Optimization**: By controlling the gate voltage and current precisely, gate drivers help optimize the performance of power devices, reducing losses and improving efficiency.

Among all the characteristics of SiC MOSFETs, the most prominent is fast switching speed. In fast switching configuration, energy in the parasitic inductance and capacitance in power path causes voltage and current overshoot and oscillation. Switching speed, generally represented by dv/dt and di/dt, largely determines the magnitude of overshoot and oscillation. Due to the superior switching speed, safety operation of SiC MOSFET is challenged by high voltage and current stress, and EMI performance is also degraded. To ensure high-performance and safe operation of SiC MOSFET, gate driver for SiC MOSFET has received widespread attention and research [100, 101].

B.1.1.3 Types of Gate Drivers

Gate drivers come in various types, each suited for different applications and requirements. The main types include voltage, current, and resonant gate drivers.Following are the types of gate drivers:

- **High-Side Drivers**: Used to drive power devices connected to a positive supply.
- **Low-Side Drivers**: Used to drive power devices connected to a negative supply.
- **Half-Bridge Drivers**: Combine both high-side and low-side drivers to control two switches in a bridge configuration.

B.1.1.3.1 Voltage Gate Drivers

Voltage gate drivers are the most common type and are used to apply a specific voltage to the gate of a power device.

B.1.1.3.2 Current Gate Drivers

Current gate drivers supply a controlled current to the gate of a power device. This type of driver is particularly useful for applications requiring precise control over the switching speed and pattern.

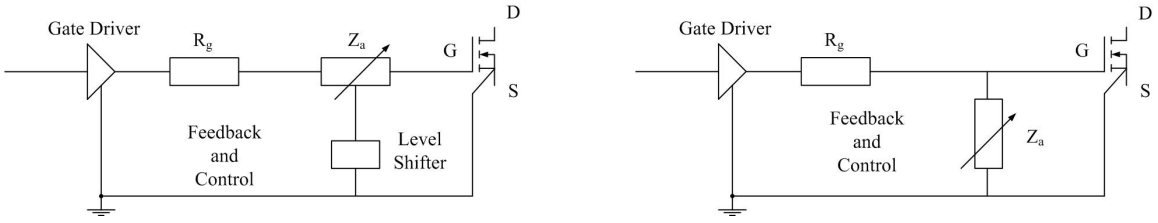
B.1.1.3.3 Resonant Gate Drivers

Resonant gate drivers use resonant circuits to drive the gate of power devices. These drivers are designed to minimize switching losses and improve efficiency by utilizing the resonance between inductance and capacitance in the circuit.

Traditionally, on/off drivers with fixed resistors are used for gate driver. This type of gate driver is often referred as conventional gate driver (CGD). The simplest is mono-resistor CGD with a single gate drive resistor. Dual resistor CGD uses different resistor

values for turn-on and turn-off. By changing the gate drive resistors, CGD has limited control of the switching speed. Due to the fixed driving strength, although CGD can change the average dv/dt and di/dt values during the switching process, the waveform patterns of current and voltage during the switching action remains consistent. Overall, CGD is restricted by the tradeoff between loss, stress, and EMI [102, 103].

Active gate driver (AGD) targets this problem generally by driving the gate with an altering voltage or current pattern during the switching process. Figure B.1.1 depicts the schematics of the different AGDs. Precisely controlled driving strength during the switching transient optimizes the switching pattern, lowering the voltage and current overshoot. Previous researches have shown a variety of AGD implementation methods. Resistor-switch array, controlled current source, controlled voltage source or any other circuitry that modulates gate drive signal can be used for driving strength control. Za is controlled impedance, which could be variable resistance, variable capacitance [104–106].



(A) Series Impedance Gate Driver (B) Parallel Impedance Gate Driver

FIGURE B.1.1: Types of Active Gate Drivers

The existing AGDs can be divided into three categories based on circuit structure. The Kelvin-source (KS) node, which is internally connected to the MOSFET's source to minimize the influence of source current for gate driver, is used as reference point for gate drivers. Using the KS node as reference point, series impedance AGD places Za in series with the gate driver, parallel impedance AGD places Za in parallel with the gate driver [107].

B.1.1.4 Current Trends in the Market for Gate Drivers

The gate driver market is evolving rapidly, driven by advancements in power electronics and increasing demand for efficient power management solutions. Recent developments in the industry have focused on dynamic gate driver circuits that significantly reduce turn-off switching losses while maintaining low cost and similar surge voltage to conventional gate drivers. Innovative gate driver designs combine multi-stage gate voltage control with feedback circuits to achieve a balance between voltage and current overshoots and switching losses. Additionally, smart gate drivers aim to integrate more protection and monitoring options, such as current and temperature sensing techniques, enhancing the reliability of the device and the inverter [108, 109].

B.1.1.4.1 Technological Innovations

Recent innovations in gate drivers include the development of integrated gate driver chips that offer enhanced performance and reliability. These chips are designed to handle higher switching frequencies and provide better thermal management.

B.1.1.4.2 Application Expansion

Gate drivers are increasingly being used in new applications such as smart grids, which require sophisticated power control systems. The demand for gate drivers in these applications is expected to continue growing, driving further advancements in the technology.

The increasing demand for high switching frequencies in power electronics is driven by the need for enhanced performance in modern applications. As reported in existing literature, operating power devices at elevated frequencies results in steeper di/dt and dv/dt transitions, primarily influenced by parasitic capacitances and stray inductances. These rapid transitions induce oscillations and overshoots in both current and voltage, which can significantly impact system stability and efficiency [110].

Adjusting the gate resistor value plays a critical role in mitigating these overshoots. A larger gate resistance effectively reduces voltage and current spikes; however, it also contributes to increased switching losses. Conversely, employing a smaller gate resistor minimizes losses but amplifies voltage and current overshoots, potentially leading to electromagnetic interference (EMI) issues and elevated stress on the semiconductor devices. Thus, achieving an optimal balance between loss reduction, transient suppression, and EMI minimization remains a critical design challenge in high-frequency applications [111].

To address these challenges, various approaches have been explored, including the application of snubber circuits in both Silicon (Si) and Silicon Carbide (SiC) devices. Snubber networks effectively suppress transient spikes but may introduce additional stress on passive components such as capacitors, and diodes.

In addition to passive solutions, significant advancements have been made in gate driver design for both Si and SiC technologies. For conventional silicon-based power devices, a range of gate driver circuits, including resonant gate drivers and Active Gate Drivers (AGD), have been developed to optimize switching characteristics. Similarly, for SiC devices—such as SiC BJTs and SiC JFETs—specialized gate drivers have been designed to account for the distinct electrical characteristics of wide-bandgap (WBG) semiconductors. Although these driver technologies are adaptable to SiC MOSFETs, specific modifications are required to accommodate differences in device behavior compared to traditional MOSFETs and IGBTs. Notably, SiC MOSFETs exhibit lower transconductance relative to silicon-based devices, necessitating higher gate–source voltage levels. Furthermore, the gate–source voltage waveform is typically asymmetrical, requiring carefully selected gate resistance (Rg) values to optimize both turn-on and turn-off transitions. Conventional two-resistance gate driver designs are commonly employed for independent control of the switching paths, though their effectiveness in balancing efficiency and EMI suppression remains limited [112–114].

The evolution of power electronics is increasingly leaning towards the development of intelligent and adaptive gate driver technologies that enhance both performance and

reliability. Innovations in this domain include real-time control over switching dynamics, integrated protection mechanisms, and enhanced compatibility with wide-bandgap (WBG) devices. These advancements are crucial for optimizing the efficiency and robustness of traction inverters and other critical power electronic systems [115, 116].

The pursuit of more sophisticated gate driver architectures continues to be a focal point in research, aimed at achieving seamless operation in high-frequency environments while minimizing losses and mitigating EMI challenges.

B.1.1.5 Gate Driver in Traction Inverter Applications

Gate drivers play a crucial role in traction inverter applications, particularly in electric vehicles (EVs) and hybrid electric vehicles (HEVs).High power-density traction inverters are being equipped with gate drivers featuring protection functions to detect excessive temperatures, over-current. Active gate drive techniques using dV/dt feedback from analog differentiators are employed to control turn-off speed, reducing surge voltage and switching losses. Wide Bandgap (WBG) devices present new challenges due to their high current densities, fast switching capabilities, and high-temperature operation. These factors impact driver ICs, which must operate at higher temperatures and ensure higher voltage isolation barriers. The fast switching behavior of WBG devices emphasizes the effects of parasitics responsible for voltage overshoot and ringing. Integrating the driver IC with the power module is a suitable solution to limit stray inductance by reducing the distance between the gate and the chip.

B.1.1.5.1 Importance in Traction Inverters

Traction inverters convert DC power from the EV battery into AC power to drive the electric motor. Gate drivers in traction inverters control the power devices (typically SiC MOSFETs or IGBTs) that perform this conversion. Gate drivers significantly influence the efficiency of the inverter by affecting the dynamic behavior of IGBTs and

freewheeling diodes. They consist of integrated circuits (ICs) that transfers isolated control signals to switch the device and provide protective feedback. For high voltage applications, such as traction inverters, optocouplers or pulse transformers are typically used for isolation. The design of gate drivers must consider factors influencing power device switching performance. Various approaches have been developed, ranging from passive circuits using external gate-emitter capacitors and gate resistors to closed-loop control that adjusts the gate drive output based on IGBT operation[117, 118].

B.1.1.5.2 Design Considerations

Designing a gate driver for traction inverters involves several considerations:

- **Temperature Management**: Gate drivers must withstand high temperatures and provide efficient thermal management.
- **Dynamic Gate Strength**: Recent innovations allow gate drivers to toggle between multiple preset current values based on EV operating conditions, optimizing the switching rate and improving overall efficiency.

B.1.2 Objective of the Thesis

The objective of this thesis is to model an advanced gate driver for traction inverter applications. The following points will be targeted in this thesis:

1. **OUT Drive**: This involves generating a basic Pulse Width Modulation (PWM) signal, which is essential for controlling the switching of the MOSFET. The PWM signal will be carefully designed to ensure efficient operation of the MOSFET, minimizing losses and optimizing performance.
2. **Implementation of Protection Features**: The gate driver model will incorporate several critical protection features to ensure safe and reliable operation. These features include:

- **AMC (Active Miller Clamp)**: This feature prevents false turn-on of the MOSFET due to Miller capacitance effects during high dv/dt conditions.
- **DESAT (Desaturation Detection)**: This protection mechanism detects over current conditions by monitoring the saturation voltage of the MOSFET, providing a rapid response to shut down the device and prevent damage.
- **OVC (Over Voltage Clamping)**: This feature protects the MOSFET from over voltage conditions by clamping the gate voltage to a safe level, ensuring the device operates within its specified limits.
- **SCP (Short Circuit Protection)**: This feature protects the MOSFET in the short circuit conditions.
- **PSTO (Programmable Soft Turning Off)**: This feature gets activated when DESAT, OCP and SCP occurs. This bring down the Vgs in a controlled manner.

3. **Hardware Implementation**: The theoretical model of the gate driver will be implemented on hardware to validate its performance. This involves designing and fabricating a prototype gate driver circuit, followed by Double Pulse Test to measure its effectiveness in real-world conditions.

B.1.3 Methodology

To achieve the objectives of this thesis, the following methodology is employed:

- **Comprehensive Study of Gate Drivers and Their Requirements**: Conduct an in-depth analysis of gate drivers, focusing on their functionalities, design considerations, and operational requirements. This includes understanding the various types of gate drivers and their applications in power electronics.
- **Protection Features Analysis and Simulation**: Investigate the protection features integrated into gate drivers, such as Under-Voltage Lockout (UVLO), Over-Voltage Lockout (OVLO), Overcurrent Protection (OCP), and Short Circuit Protection

(SCP). Simulate these protection mechanisms to gain a thorough understanding of their operation and effectiveness in safeguarding the system.

- **Double Pulse Test**: Perform a double pulse test on the gate driver IC to evaluate its performance and correctness. This test is crucial for assessing the dynamic behavior of the gate driver, including its switching characteristics and response to transient conditions.

By following this methodology, the thesis aims to provide a comprehensive understanding of gate driver design, simulation, and testing, ensuring the development of robust and efficient gate drivers for traction inverter applications.

B.1.4 Outline of Annexure

The annexure is organized as follows:

- **Chapter 2B: Double Pulse Test**

  This chapter discusses the double pulse test, which is essential for the characterization of MOSFETs. The double pulse test is crucial for understanding the switching behavior and performance of MOSFETs under various conditions. This chapter lays the foundation for subsequent chapters, as all important protection features are tested using this double pulse test model.

- **Chapter 3B: Output Drive of the Gate Driver**

  This chapter provides an in-depth analysis of PWM generation by the gate driver, which is vital for driving MOSFETs. It explores the different current capabilities of the gate driver and how it drives the MOSFET through output selection. Understanding PWM generation is key to optimizing the performance of the gate driver.

- **Chapter 4B: Protection Features in Gate Driver**

  This chapter details the various protection features required for a gate driver in

traction inverter applications. It covers mechanisms such as DESAT, Active Miller Clamp and Over Voltage Clamp (OVC). These features are essential for safeguarding the gate driver and ensuring reliable operation under different conditions.

- **Chapter 5B: Programmable Soft Turning Off**

  This chapter discusses the concept of programmable soft turning off (PSTO), which is activated when protection features are triggered. It explains the necessity of PSTO, its implementation process, and how it contributes to the overall protection strategy of the gate driver.

- **Chapter 6B: UVLO, OVLO, OCP, and SCP**

  This chapter provides a comprehensive overview of Under-Voltage Lockout (UVLO), Over-Voltage Lockout (OVLO), Overcurrent Protection (OCP), and Short Circuit Protection (SCP) available in the gate driver. It discusses the principles, implementation, and significance of these protection mechanisms in ensuring the safe operation of the gate driver.

- **Chapter 7B: Hardware Implementation**

  This chapter focuses on the hardware implementation of the double pulse test conducted on the gate driver IC. It presents the experimental setup, and results obtained from the hardware tests.

DOUBLE PULSE TEST

B.2.1 Introduction to DPT

A double pulse test (DPT) is commonly used for the characterization of power electronic devices, such as MOSFETs and IGBTs. Typically, the device datasheet provides detailed information about the device under specific operating conditions. However, these conditions may differ from the user-specific application conditions. A DPT setup assists in characterizing a power electronic device under user-specific conditions. Additionally, it aids in the experimental estimation of device losses and the testing of gate driver protections.

B.2.1.1 Significance of DPT

For the reliability of IGBT/MOSFET devices, the double pulse test (DPT) is a standard tool that can be used for the above purpose. For a reliable operation, a good engineering practice is to test the gate driver for these protection mechanisms. A DPT setup can help test the gate driver also.

Although the IGBT datasheet may provide detailed information, the test parameters such as DC-bus voltage, collector current, gate resistor, and junction temperature used in the datasheet may be different from the user operating conditions. In order to have an early understanding of the device characteristics at the user-specific operating conditions, DPT tests become essential. Experimental waveforms from DPT tests allow accurate estimation of device losses, aiding in the appropriate sizing of heat sinks for reliable operation. Furthermore, DPT setups evaluate gate driver protections, which are crucial for device reliability in power electronic converters. Apart from the primary function of providing an isolated communication channel between the controller and the device, the gate driver continuously monitors the device voltages (collector emitter voltage and gate

emitter voltage) in order to detect abnormal operation. Once an anomaly is detected, the gate driver should seize the device operation in order to protect it from permanent failure. Therefore, it is imperative to test the device and the gate driver using a DPT setup before installing in a power converter [119].

B.2.1.2 Advantages of DPT

The performance of switching devices significantly impacts the operating frequency and loss of power electronic circuits. Therefore, testing the working characteristics of these devices using a double pulse test is necessary. Factors affecting device performance include parasitic capacitance and inductance in the device and the working circuit. Test methods, such as DPT, are preferred over modeling and simulation because they do not require extracting parasitic parameters and are closer to actual application conditions. The double pulse test is a well-established method for determining the turn-on delay time, rise time, turn-off delay time, and fall time of switching devices. Additionally, it measures the recovery current amplitude and change rate of the reverse parallel diode [120].

B.2.1.3 Simulation of DPT on module

A simulation was conducted on a Wolfspeed MOSFET half-bridge using the SIMetrix software. Figure B.2.1 illustrates the simulation diagram of the setup. An inductor is connected to the high side of the half-bridge, and the gate to source is shorted in accordance with DPT standards. When a pulse is applied to the low-voltage side MOSFET, the current through the inductor increases. Once the pulse is removed, the current through the inductor freewheels through the diode of the High side MOSFET. Upon applying another pulse, the current rises again, achieving the desired current in this process. During turning ON and OFF of the MOSFET, the switching energy is lost which is calculated.

Figure B.2.2 depicts the simulation results of the DPT. Figure B.2.2a depicts the rise in voltage and current when the DPT is performed. Along with that the power and the

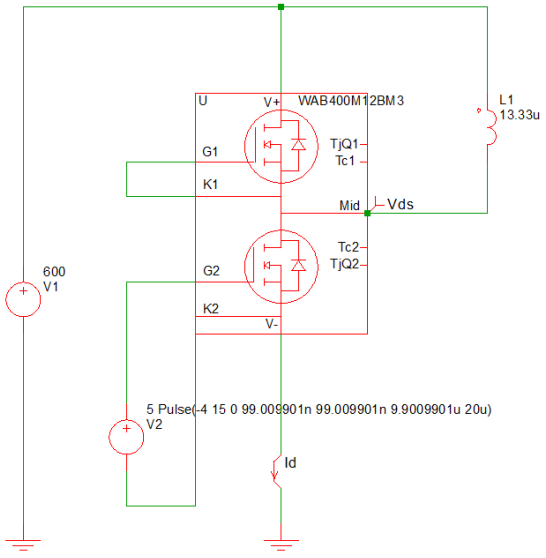


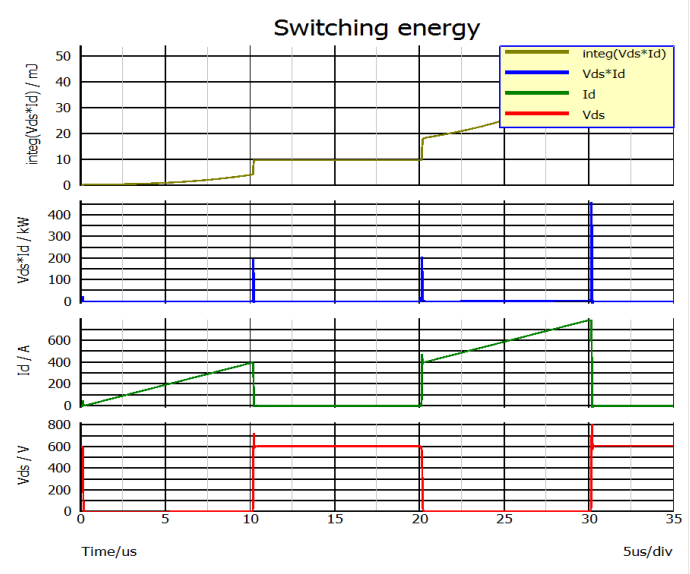
FIGURE B.2.1: Simulation Model for DPT

switching energy loss is also calculated. Figure B.2.2b shows the comparative analysis of the switching energy loss during turn ON and turn OFF which matches with the graph given in the datasheet.

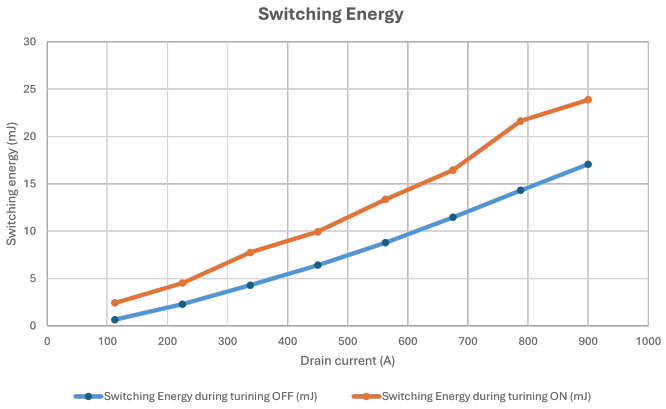
B.2.2 Conclusion

This chapter provided a comprehensive overview of the Double Pulse Test (DPT) methodology, along with detailed simulation results. The results obtained were consistent with the expectations and aligned well with the datasheet specifications of the Wolfspeed model. This validation underscores the accuracy and reliability of the simulation process.

Moreover, this chapter serves as a foundational reference for testing various protection features. The insights gained from the DPT are crucial for understanding the behavior of the device under different conditions, making it an indispensable tool for ensuring robust protection mechanisms. The role of DPT in evaluating and enhancing protection features cannot be overstated, as it provides critical data that informs the design and implementation of effective protection strategies.



(A) Switching Energy Loss Calculation


Switching Energy
Switching energy (mJ)
Drain current (A)
Switching Energy during turining OFF (mJ)
Switching Energy during turining ON (mJ)

(B) Switching Loss for Turning ON and OFF

FIGURE B.2.2: Simulation Result for the DPT

In summary, the DPT not only validates the performance of the device but also plays a pivotal role in the development and testing of protection features, ensuring the overall reliability and safety of the system.

OUT DRIVE OF GATE DRIVER

B.3.1 Introduction

Traction inverters are essential components in electric vehicle (EV) powertrains, responsible for converting DC power from the battery into AC power for driving electric motors. A key aspect of traction inverter performance lies in the gate driver circuitry, which governs the switching behavior of power transistors, typically IGBTs. Gate drive control is crucial to ensure accurate PWM, minimize switching losses, and improve overall system reliability.

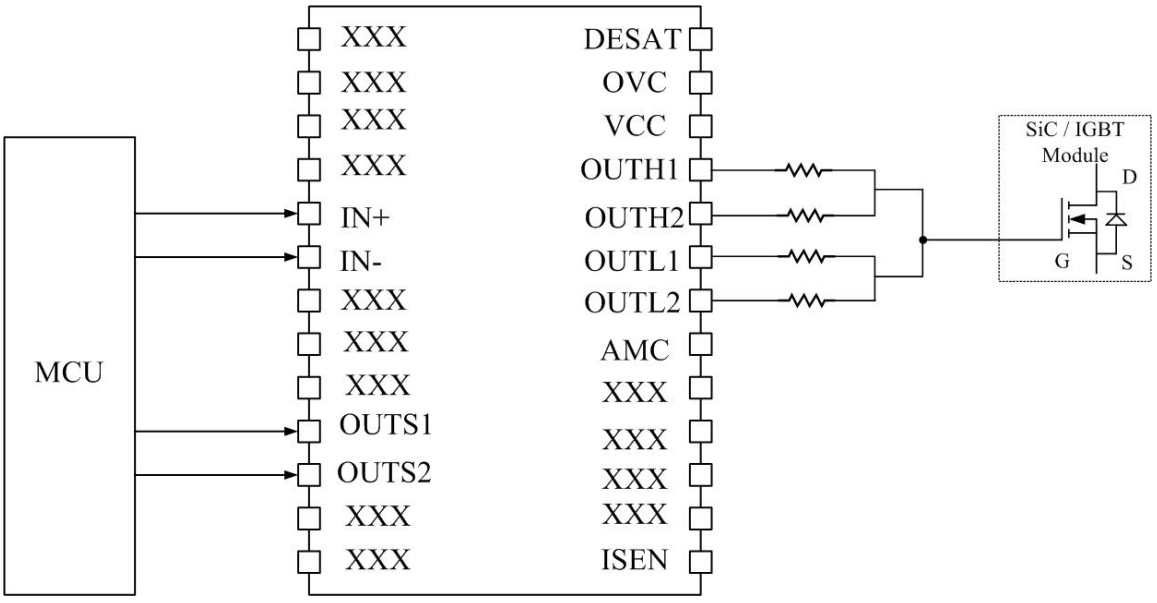


FIGURE B.3.1: Application Schematic

Figure B.3.1 depicts the application diagram in which some of the input and output pins of the IC are mentioned. One of the significant gate driver features utilized in traction inverters is the implementation of driver source and sink networks, OUTH and OUTL respectively. These mechanisms are integrated in high-performance gate drivers, to provide robust switching capabilities. OUTH and OUTL ensure reliable gate drive voltage levels by dynamically pulling the gate output to high state and -VEE (low state), respectively. This precise control over gate voltage significantly impacts the generation and stabilization of

PWM pulses. The IN+ and IN- signals are generated by the micro-controller which is controlling the traction inverter.

The following sections detail the architecture and design of OUTH and OUTL, explain their working principles, and discuss the key advantages of employing this configuration in traction inverters.

B.3.2 Architecture and Design of OUTH and OUTL

The gate driver architecture for traction inverters employs OUTH and OUTL as critical output nodes for controlling the power transistor gate voltage. These nodes are responsible for delivering a well-defined gate drive voltage swing to ensure the proper switching of the IGBT or MOSFET.

B.3.2.1 Gate Voltage Control

The OUTH pin is configured to pull the gate voltage up to +20V by monitoring the IN+ and IN- signals, ensuring full enhancement of the power device. Conversely, the OUTL pin pulls the gate voltage down to -VEE, guaranteeing fast and reliable turn-off. The gate voltage thus generated will drive the MOSFET/IGBT with proper voltage and there will not be any shoot through.

B.3.2.2 PWM Pulse Generation

Figure B.3.2 illustrates the block diagram for the OUTH and OUTL blocks. A 3.3V signal is generated by the microcontroller and fed through the IC as IN+ and IN- signals. Upon receiving the IN+ and IN- signals, it is given to the level shifter. Consequently, the OUTH pin is pulled to VCC, and the OUTL pin is pulled to VEE, facilitated by the internal MOSFETs. This process results in the generation of pulses for the external MOSFETs. In this manner a pulse is obtained at the OUTH and OUTL pin that will be able to drive the

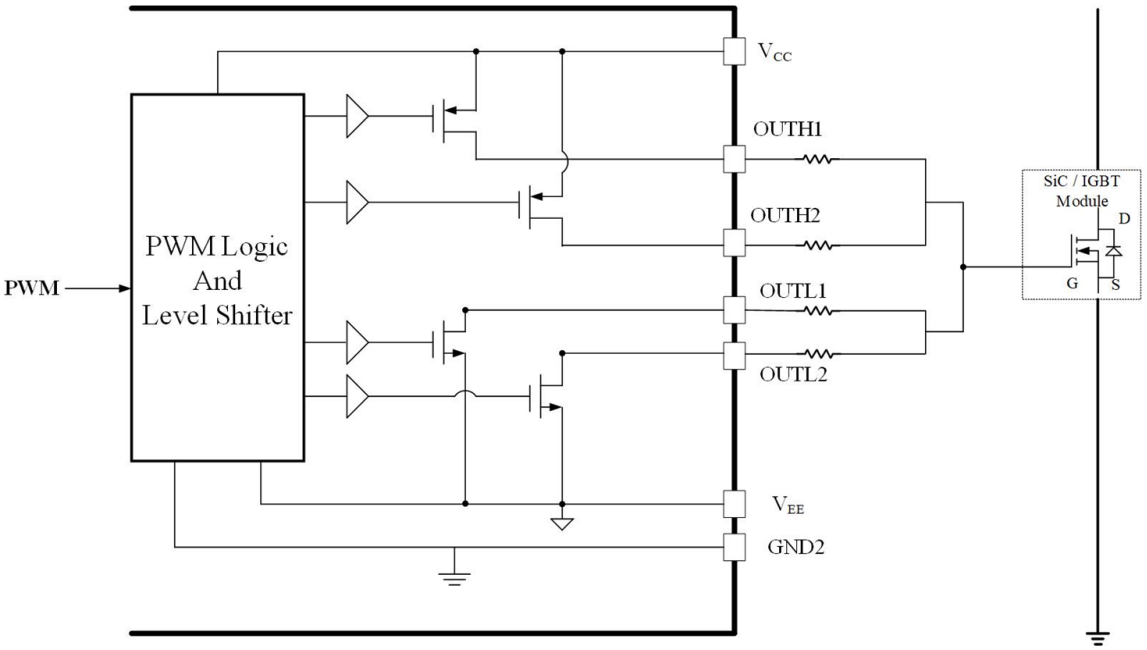


FIGURE B.3.2: Block Diagram for OUTH and OUTL

MOSFET/IGBT module. The VEE which is a negative bias is the configurable parameter in the gate driver. During the turnoff process the gate is pulled down to this negative bias value. By this principal of OUTH and OUTL, gate driver handles high switching frequencies and large current demands typical of traction inverters. This driver are designed to withstand harsh automotive environments, providing robust isolation, fault detection, and overvoltage and overcurrrent protection. The integrated approach reduces the need for external components and enhances the power density of the inverter system.

B.3.3 Implementation Through Simulation

Figure B.3.3 presents the simulation diagram that drives a MOSFET through the OUTH and OUTL pins. The process begins with the IN+ and IN- signals, which are obtained from the microcontroller. The PWM logic is responsible for generating the appropriate signal.

In this simulation, a voltage-controlled switch is utilized, incorporating the appropriate resistance to ensure accurate operation. The generated PWM signal effectively drives the

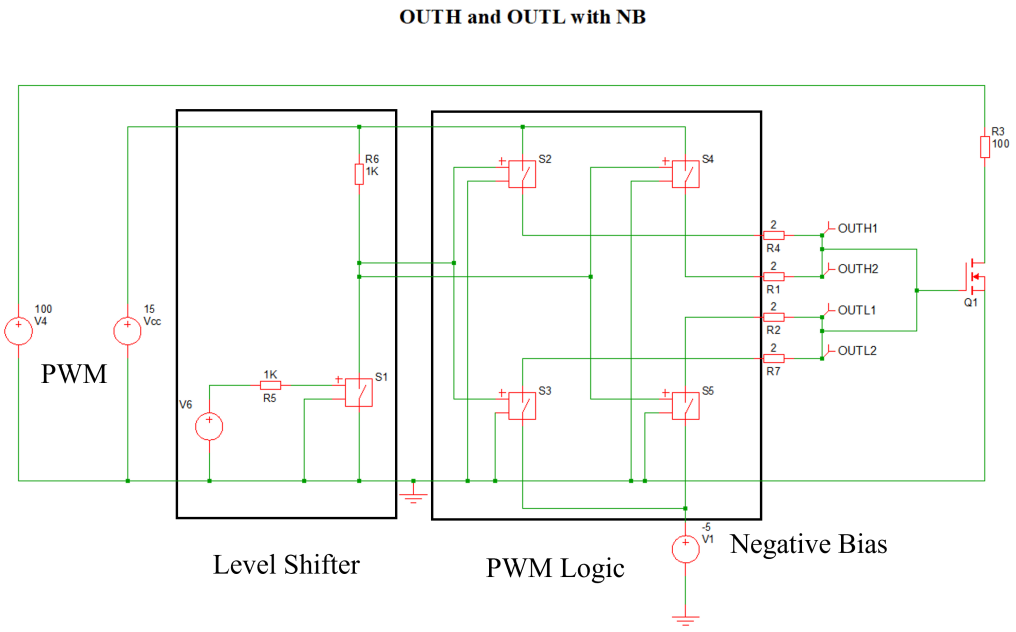


FIGURE B.3.3: Simulation Diagram for OUTH and OUTL

MOSFET, demonstrating the interaction between the various components and the overall functionality of the system.

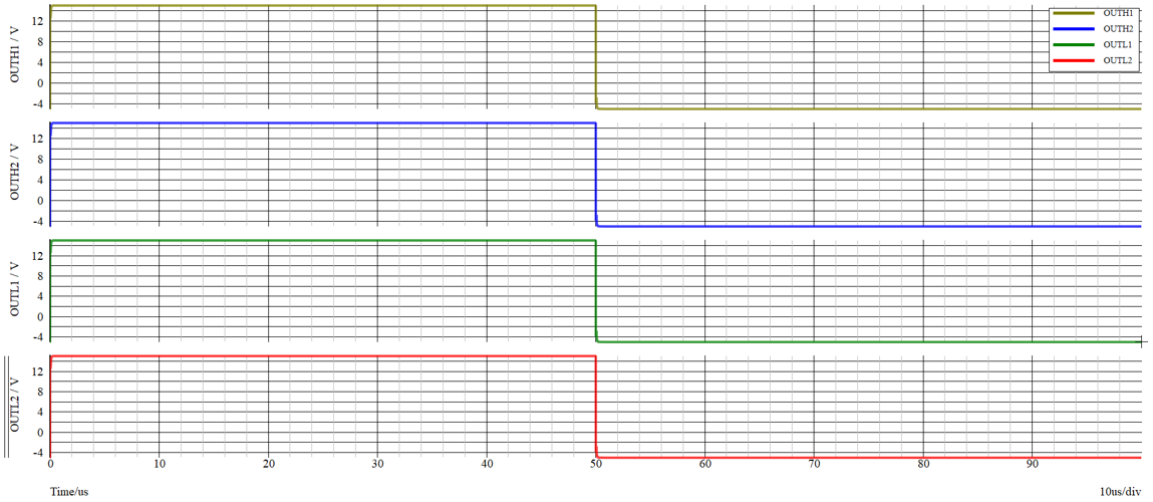


FIGURE B.3.4: Simulation Result for OUTH and OUTL

Figure B.3.4 depicts the results obtained from the OUTH and OUTL pins. The gate is pulled to +15V and to the negative bias level of -5V. As the complete mechanism of the OUTH and OUTL pins drives the system, the PWM waveform is generated at all four pins, which can be observed in the simulation results.

B.3.4 Advantages of OUTH and OUTL in Traction Inverters

The use of OUTH and OUTL configurations in traction inverters offers several advantages:

- **Enhanced Switching Efficiency:** By providing a +20V gate voltage during ON states and -VEE during OFF states, switching losses are significantly reduced, leading to lower heat generation.
- **Improved Power Density:** Compact gate driver design with integrated OUTH and OUTL reduces the number of external components, enhancing the overall power density of the traction inverter.
- **Faster Turn-On and Turn-Off:** The robust voltage swing facilitates rapid switching, essential for maintaining high-frequency PWM signals.
- **Reduced Thermal Stress:** Precise voltage control minimizes switching spikes and reduces power dissipation, enhancing thermal stability.
- **Controlled Turn On and Off**: By implementing this feature a controlled turn On and Off is achieved.

B.3.4.1 Conclusion

In traction inverter applications, the combination of OUTH and OUTL gate drive configurations significantly enhances the performance of power transistors by reducing switching losses and maintaining efficient gate voltage control. The adoption of this gate driver technology in traction systems demonstrates a reliable, compact, and thermally efficient solution for modern electric vehicle powertrains. To accommodate different current capabilities, the gate driver includes the features OUTS1 and OUTS2, which determine the current values passing through the OUTH and OUTL pins.

B.3.5 Need for OUTS1 and OUTS2

The gate driver architecture for traction inverters incorporates OUTS1 and OUTS2 as critical nodes responsible for current modulation during switching events. Various modules of Insulated Gate Bipolar Transistors (IGBTs) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are available for traction inverter applications. Given the differing driving strengths of each module, it is essential to accommodate these variations within the gate driver to ensure compatibility and optimal performance across different modules. To achieve this, the OUTS1 and OUTS2 pins play a crucial role.

OUTS1 and OUTS2 are input pins located on the input side of the integrated circuit (IC). The microcontroller, which generates the IN+ and IN- signals, also provides signals to these pins, facilitating the selection of the appropriate current limit. Table B.3.1 enumerates the different current ratings available for selection. Additionally, the configuration register is involved in this decision-making process. The configuration register can be set through a graphical user interface (GUI), allowing for precise adjustments to meet the specific requirements of the application.

TABLE B.3.1: Out Drive Strength

Configuration	OUTS1	OUTS2	OUTH1	OUTH2	OUTL1	OUTL2
[OUT_I] = 0	0	0	5A	0A	5A	0A
	0	1	5A	0A	5A	10A
	1	0	5A	10A	5A	0A
	1	1	5A	10A	5A	10A
[OUT_I] = 1	0	0	0A	0A	5A	0A
	0	1	0A	0A	5A	10A
	1	0	0A	10A	5A	0A
	1	1	0A	10A	5A	10A

B.3.5.1 Simulation Implementation

The OUTS1 and OUTS2 features of the integrated circuit (IC) were simulated using SIMertix software, and the results were documented accordingly. Figure B.3.5 illustrates

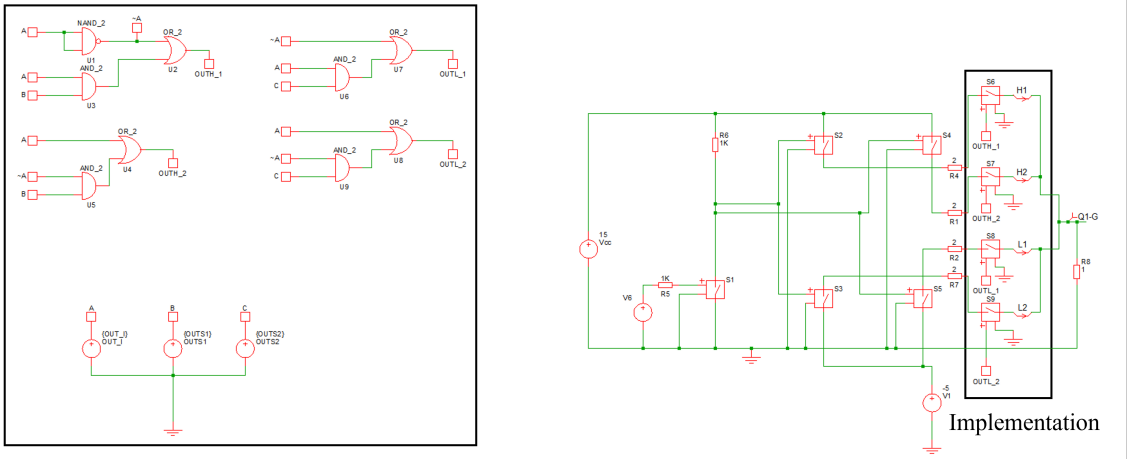


FIGURE B.3.5: Current Modulation in Gate Driver using OUTS1 and OUTS2

the simulation diagram for these features. A logic, based on the specified table, is generated through basic gates, which are implemented within the IC. By controlling the programmable parameters, a current setting is established and applied to the voltage-controlled switch, which emulates the MOSFET within the IC. This implementation is integrated into the OUTH and OUTL configuration to achieve precise current control.

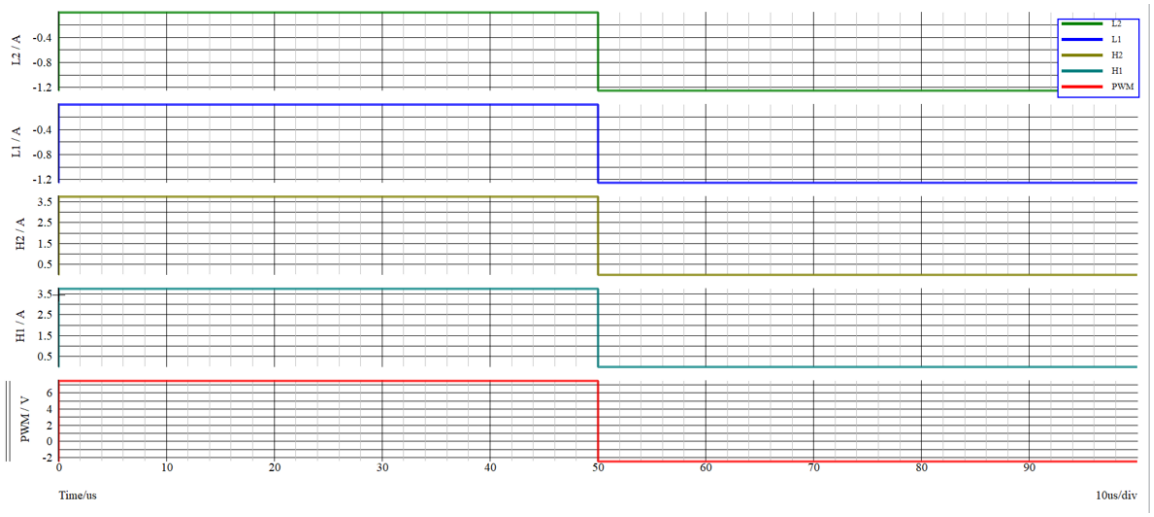


FIGURE B.3.6: Simulation Result for OUTS1 and OUTS2

Figure B.3.6 presents the results of the simulation, demonstrating the various current levels obtained. These current ratings reflect the full strength of the gate driver. The

simulation results confirm the successful implementation of the feature, which facilitates current selection through the primary side pins.

The simulation was conducted to evaluate the performance of the OUTS1 and OUTS2 features under different conditions. The results indicate that the gate driver can effectively modulate the current levels, ensuring optimal performance across a range of operating scenarios. The ability to select and control current through the primary side pins is crucial for adapting to different module requirements, thereby enhancing the versatility and robustness of the gate driver.

The detailed analysis of the simulation results shows that the current levels are consistent with the expected values, validating the design and implementation of the OUTS1 and OUTS2 features. This successful simulation underscores the importance of these features in providing precise current control, which is essential for the reliable operation of the gate driver in traction inverter applications.

B.3.6 Conclusion

This chapter serves as the fundamental building block of the gate driver. It explains the generation of Pulse Width Modulation (PWM) signals and the control of current through the output pins according to specific requirements. By implementing these features, the gate driver can accommodate different MOSFET and IGBT modules.

In conclusion, this chapter establishes the foundational concepts necessary for understanding the gate driver's operation. With the basic building blocks clarified, the subsequent chapter will delve into the various protection features integrated into this gate driver.

PROTECTION FEATURES IN GATE DRIVER

B.4.1 Introduction to Protection Features of Traction Inverter

In modern EV powertrains, traction inverters serve as the critical interface between the high-voltage battery and the electric motor. The primary protection features integrated into traction inverters include Desaturation (DESAT) Protection, Active Miller Clamping (AMC), and Overvoltage Protection (OVC).

1. Desaturation (DESAT) Protection: This mechanism is widely utilized for short-circuit protection in IGBT and SiC MOSFETs. DESAT protection monitors the voltage across the power semiconductor during operation. If the voltage exceeds a predefined threshold, indicating a potential short circuit, the protective circuit is triggered to turn off the device safely. This method is cost-effective and provides rapid response to fault conditions, ensuring device safety and longevity.

2. Active Miller Clamping (AMC): Active Miller Clamping (AMC) is designed to prevent unintended turn-on of IGBT/ MOSFET during high dv/dt transients. AMC effectively clamps the gate voltage during the off-state, thereby preventing spurious turn-on and significantly enhancing system reliability.

This feature is of paramount importance in avoiding shoot-through conditions, which can occur when both the high-side and low-side switches conduct simultaneously, leading to catastrophic failure. By ensuring that the gate voltage remains stable during critical switching periods, AMC plays a crucial role in maintaining the integrity and performance of the power electronics system.

3. Over Voltage Clamping (OVC): To prevent damage caused by voltage transients, traction inverters employ Over Voltage Clamping (OVC). This feature monitors the DC

link voltage and responds rapidly to over voltage conditions by clamping the voltage to the predefined value. OVC protects critical inverter's MOSFET/IGBT module from excessive voltage stress, thereby improving system durability.

These protection mechanisms work in tandem to maintain the stability and reliability of traction inverters under various operating conditions. In the following sections, each of these protection features is explored in detail, highlighting their design principles, operation, and contributions to electric vehicle safety.

B.4.2 Introduction to DESAT Protection

Desaturation (DESAT) detection is a well-established method for short-circuit protection in power semiconductor devices, particularly in IGBT and MOSFETs. The growing adoption of SiC technology in high-power applications is primarily due to its high-speed switching capabilities and low conduction losses. However, these advantages come with the drawback of reduced short-circuit withstand capability, necessitating robust protection mechanisms.

Desaturation (DESAT) protection take into consideration the voltage across the device's terminals. When the voltage exceeds a predefined threshold while the gate remains active, a desaturation condition is detected, indicating a potential short circuit. This triggers the protective circuitry to safely turn off the device, thereby preventing catastrophic damage.

Compared to current transformers, DESAT protection is cost-effective, reliable, and straightforward to implement, making it highly suitable for high-performance power applications. Implementing DESAT protection is economically advantageous due to the lower cost and ease of integration of the required components [116].

B.4.2.1 Basic Operation of DESAT Protection

The DESAT protection mechanism operates by continuously sensing the voltage across the switching device. In IGBTs, desaturation is detected when the collector-emitter voltage (VCE) significantly exceeds its nominal value, indicating excessive current flow. In SiC MOSFETs, a similar effect occurs, with desaturation resulting in a transition from the linear region to the saturation region.

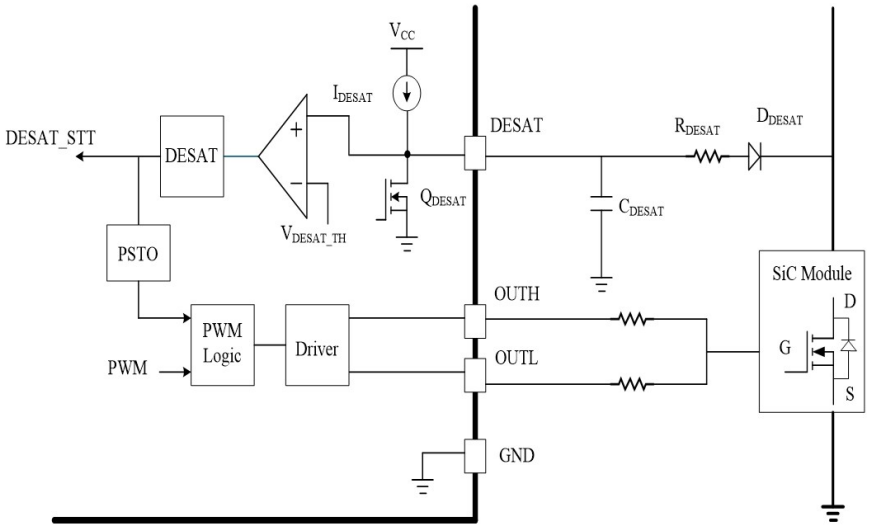


FIGURE B.4.1: Block Diagram for DESAT

DESAT circuits typically include a monitoring diode and filtering components that allow effective sensing of voltage spikes. To avoid false detection during the initial turn-on transient, a blanking time is introduced. This delay ensures that short-term voltage fluctuations do not trigger false alarms. Additionally, parameters such as detection threshold voltage and noise filter width are critical for fine-tuning the DESAT mechanism to achieve fast and reliable short-circuit detection. Figure B.4.1 represents the internal block diagram implemented to achieve DESAT protection. When the voltage exceeds a predefined threshold, the diode D_{DESAT} becomes forward-biased, causing the voltage to appear on the DESAT pin. The current, which is grounded through Q_{DESAT}, charges the external blanking capacitor. This value is then compared by the internal comparator to the configurable threshold. Upon reaching the threshold, the DESAT block

is activated, and a signal is sent to the Programmable Soft Turning Off (PSTO) block to reduce the gate voltage to VEE.

B.4.2.2 Timing Diagram

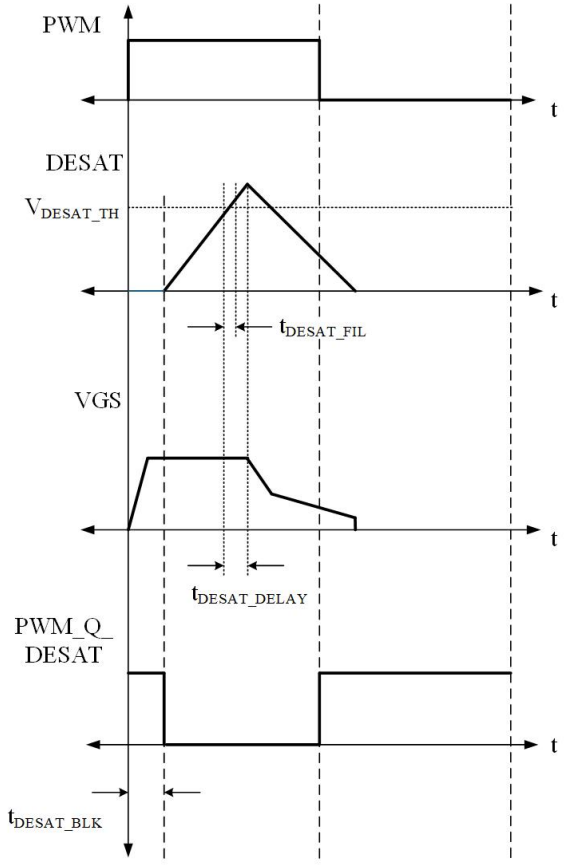


FIGURE B.4.2: DESAT Timing Diagram

Figure B.4.2 illustrates the timing diagram that depicts the various timings associated with the DESAT operation. This timing diagram outlines the critical intervals that must be considered when DESAT protection is enabled. The protection mechanism is activated when the voltage reaches a predetermined value.

During the turn-on phase, a blanking time is introduced to prevent false activation of the DESAT protection. Once the voltage at the DESAT pin reaches the threshold, a filtering time is applied to avoid any false triggers. These measures ensure the reliable and accurate operation of the DESAT protection feature.

One of the primary challenges in DESAT implementation for SiC devices is their lower short-circuit withstand time compared to conventional IGBTs. As a result, the blanking time, threshold voltage, and filter width must be precisely calibrated to ensure effective protection. If the blanking time is too long, the device may fail before protection is activated. Conversely, if it is too short, noise or transient spikes may cause false triggering. Hence, careful design consideration is crucial for reliable operation.

B.4.2.3 Simulation of DESAT

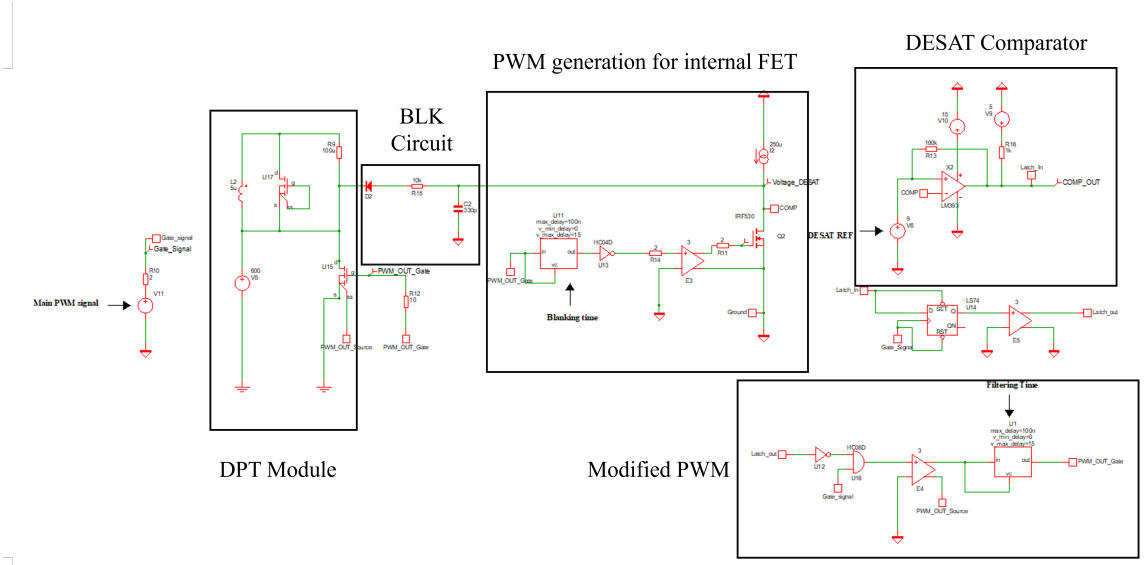


FIGURE B.4.3: DESAT Simulation Diagram

Figure B.4.3 represents the simulation diagram in which all components are integrated. A Double Pulse Test (DPT) setup is established to test the DESAT protection. The blanking circuit is constructed from various components, and a Pulse Width Modulation (PWM) generation block is created for the internal MOSFET. A DESAT comparator is present to provide a trigger when the DESAT voltage reaches the threshold. Consequently, the PWM signal is modified accordingly.

The simulation diagram incorporates all necessary elements to evaluate the DESAT protection mechanism effectively. The DPT setup ensures accurate testing conditions, while the blanking circuit prevents false activation. The PWM generation block simulates

the behavior of the internal MOSFET, and the DESAT comparator ensures precise triggering based on the voltage threshold. This comprehensive simulation setup validates the functionality and reliability of the DESAT protection feature. Figure B.4.4 presents

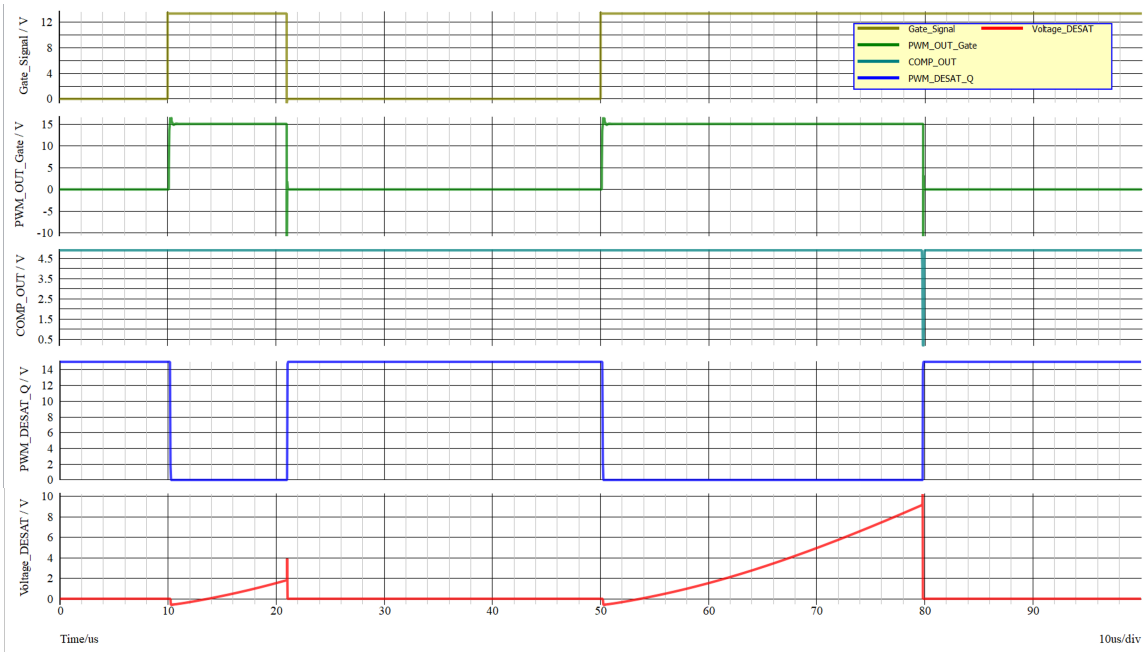


FIGURE B.4.4: Simulation Result for DESAT Feature

the output of the simulation conducted. Two distinct pulses of varying durations are provided through the source connected in the Double Pulse Test (DPT) setup. The first pulse is intentionally shorter to demonstrate that the DESAT protection is not triggered. In contrast, the second pulse, which has a longer duration, triggers the DESAT protection, causing the PWM pulse supplied to the MOSFET to be pulled low.

This simulation output effectively illustrates the functionality of the DESAT protection mechanism. The shorter pulse confirms the absence of false triggering, while the longer pulse validates the activation of DESAT protection under appropriate conditions. The modification of the PWM pulse in response to the DESAT trigger ensures the reliable operation of the MOSFET, thereby enhancing the overall system's safety and performance.

B.4.2.4 Advantages of DESAT Protection

DESAT protection offers several advantages, particularly in applications involving SiC MOSFETs and IGBTs:

- **Cost-Effectiveness:** Requires only a diode and a few passive components, making it significantly more affordable than current-sensing methods like hall sensors or transformers.
- **Simplicity of Implementation:** The design integrates seamlessly into existing gate driver circuits without extensive modifications.
- **Enhanced Device Longevity:** By preventing electrical stress during fault conditions, DESAT protection contributes to extending the life of power semiconductor devices.

The simplicity, cost-effectiveness, and reliability of DESAT protection make it an ideal choice for safeguarding SiC MOSFETs and IGBTs in high-voltage, high-speed switching applications.

B.4.3 Introduction to Active Miller Clamping (AMC)

Active Miller Clamping (AMC) is a crucial protection mechanism implemented in gate drivers for MOSFETs and IGBTs to mitigate the effects of parasitic turn-on caused by Miller capacitance during high dv/dt transients. In bridge-leg configurations, SiC MOSFETs often experience undesired gate-source voltages, commonly referred to as crosstalk voltages, during the switching intervals of complementary devices. These crosstalk voltages arise due to the displacement currents generated through the Miller capacitance (CGD) when high dv/dt is applied across the device terminals. If left unchecked, this can inadvertently trigger the OFF-state device, leading to increased switching losses, excessive current stress, and potential damage to power modules.

To address this, Active Miller Clamping actively controls the gate voltage during the OFF state of the device, preventing unintended turn-on. When the high-side switch in a half-bridge turns on, the output voltage ramps up with a high dv/dt. This generates a displacement current across CGC, increasing the gate voltage of the low-side device. If this induced gate voltage surpasses the device's threshold voltage, it may turn on unintentionally, causing cross-conduction and significant current spikes. AMC effectively prevents this by clamping the gate voltage during the critical turn-off phase, ensuring system stability and protecting the device from parasitic turn-on [121].

B.4.3.1 Working Principle of Active Miller Clamping

The working principle of AMC revolves around dynamically controlling the gate voltage during switching transients. When the IGBT or MOSFET transitions to the OFF state, the gate driver detects the potential for a Miller-induced voltage spike. To counteract this, the AMC circuit engages, providing a low-impedance path for the Miller current to discharge safely. This action is particularly crucial during high dv/dt events, where the gate voltage may be forced to rise despite the device being commanded off.

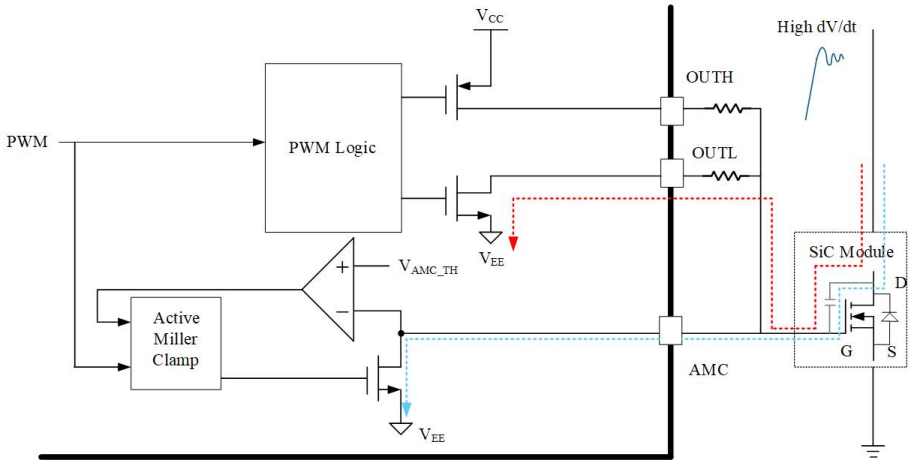


FIGURE B.4.5: Block Diagram of Active Miller Clamping (AMC)

Figure B.4.5 represents the block diagram of the Active Miller Clamping (AMC) implemented in the integrated circuit (IC). During the switching of the upper MOSFET/IGBT, the path indicated by the red line in the diagram is followed by the

current, which can be interpreted by the lower MOSFET/IGBT as a turn-on command. To prevent this unintended turn-on, the lower impedance path indicated by the blue line is provided.

The AMC mechanism ensures that the gate voltage of the lower MOSFET/IGBT remains stable during high dv/dt transients, thereby enhancing system reliability and preventing shoot-through conditions. This implementation is crucial for maintaining the integrity and performance of the power electronics system.

The Miller current, represented by:

$$I_{gc} = C_{gc} \cdot \frac{dv}{dt} \tag{38}$$

flows through the parasitic capacitance (C_{GC}) during the switching event. AMC circuits actively clamp the gate to prevent this voltage from reaching the threshold level that would trigger the device.

B.4.3.2 Timing Diagram for AMC

Figure B.4.6 depicts the timing diagram for the (AMC) feature. In this diagram, the PWM is generated for the AMC Field-Effect Transistor (FET) present in the integrated circuit (IC). The AMC FET is turned off when the other MOSFET is turned on. Due to the high dv/dt during the switching of the other MOSFET, this arrangement is necessary. When the AMC is activated, the gate-source voltage (V_{gs}) is pulled down to a low value.

This timing diagram illustrates the precise intervals and conditions under which the AMC operates, ensuring that the gate voltage remains stable and preventing unintended turn-on of the MOSFET. The implementation of AMC is crucial for maintaining system reliability and avoiding shoot-through conditions during high dv/dt transients.

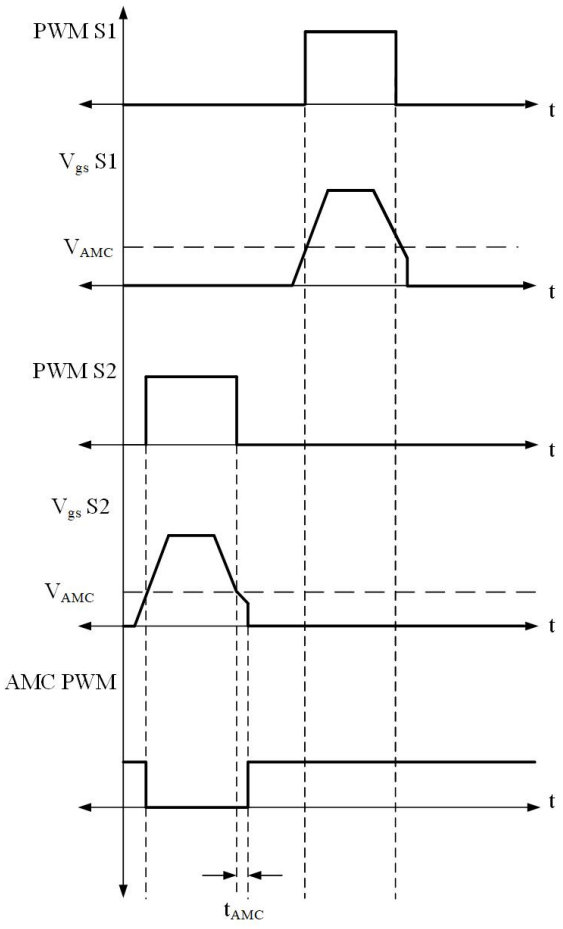


FIGURE B.4.6: Timing Diagram of Active Miller Clamping during dv/dt Events

The timing diagram also includes specific intervals designed to prevent false tripping due to erroneous triggers. The PWM signal is modified accordingly to ensure accurate operation and to avoid any unintended activation.

B.4.3.3 Simulation of AMC

Figure B.4.7 represents the simulation for the Active Miller Clamping (AMC). A Double Pulse Test (DPT) model is considered, and the Pulse Width Modulation (PWM) signals are generated to ensure proper operation in accordance with the timing diagram and functionality. The simple logic for the generation of the AMC Field-Effect Transistor (FET) is provided.

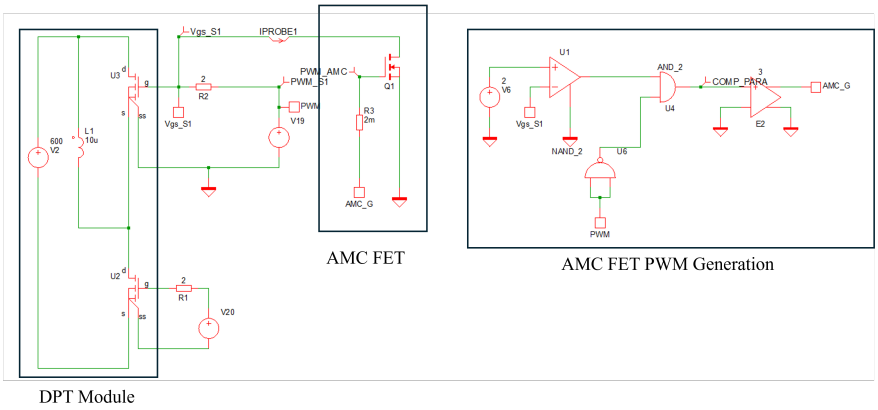


FIGURE B.4.7: Simulation Results of AMC Circuit Preventing Parasitic Turn-On

The timing diagram also includes specific intervals designed to prevent false tripping due to erroneous triggers. The PWM signal is modified accordingly to ensure accurate operation and to avoid any unintended activation.

This simulation setup validates the AMC feature by demonstrating its effectiveness in preventing unintended turn-on of the MOSFET during high dv/dt transients. The DPT model ensures that the AMC operates correctly under various conditions, and the logic for generating the AMC FET is straightforward yet effective. This comprehensive simulation confirms the reliability and robustness of the AMC implementation. Figure B.4.8 depicts

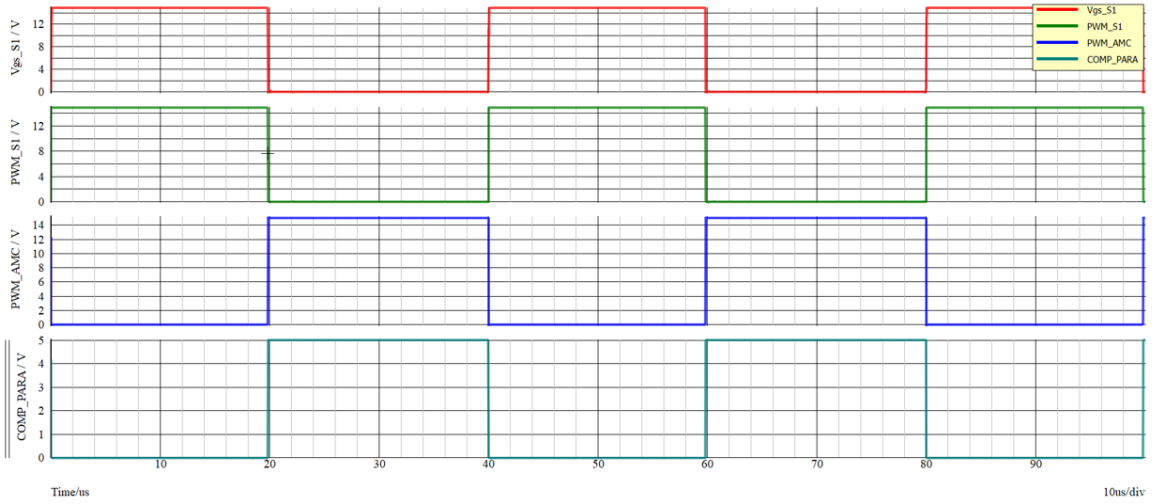


FIGURE B.4.8: Simulation Result for AMC Feature

the output of the simulation, which considers the PWM generation for the AMC FET

along with the modification of the PWM. The comparator, which is implemented as a programmable parameter, is also taken into consideration while making changes to the PWM. The PWM generated for the internal FET is shown in the output of this result.

The timing diagram also includes specific intervals designed to prevent false tripping due to erroneous triggers. The PWM signal is modified accordingly to ensure accurate operation and to avoid any unintended activation.

This simulation output validates the effectiveness of the AMC feature by demonstrating its ability to prevent unintended turn-on of the MOSFET during high dv/dt transients. The consideration of the comparator and the programmable parameters ensures that the PWM signal is accurately adjusted, thereby enhancing the reliability and robustness of the AMC implementation. The results confirm that the AMC operates correctly under various conditions, providing a comprehensive validation of its functionality.

Active Miller Clamping enhances the reliability of SiC MOSFETs and IGBTs in high-speed switching applications, effectively preventing unwanted turn-on and minimizing the risk of cross-conduction in bridge-leg configurations. Its integration into gate driver circuits significantly reduces switching losses, enhances thermal stability, and extends the operational life of power modules.

B.4.4 Introduction to Overvoltage Clamping (OVC)

Over voltage Clamping (OVC) is a critical protection mechanism employed in gate drivers to prevent excessive voltage stress across the drain-source terminals (Vds) of power semiconductors such as MOSFETs and IGBTs. During switching transients, high-speed commutation can induce voltage overshoot across the device, potentially exceeding its rated Vds voltage. This overvoltage condition can lead to breakdown and permanent damage if not mitigated effectively.

The OVC mechanism is designed to monitor the Vds voltage and activate a clamping circuit when a predefined voltage threshold is surpassed. This clamping action rapidly absorbs the excess energy, limiting the voltage spike and preventing it from reaching destructive levels. By integrating OVC directly into the gate driver, the switching device is protected from transient overvoltage events, ensuring long-term reliability and safety.

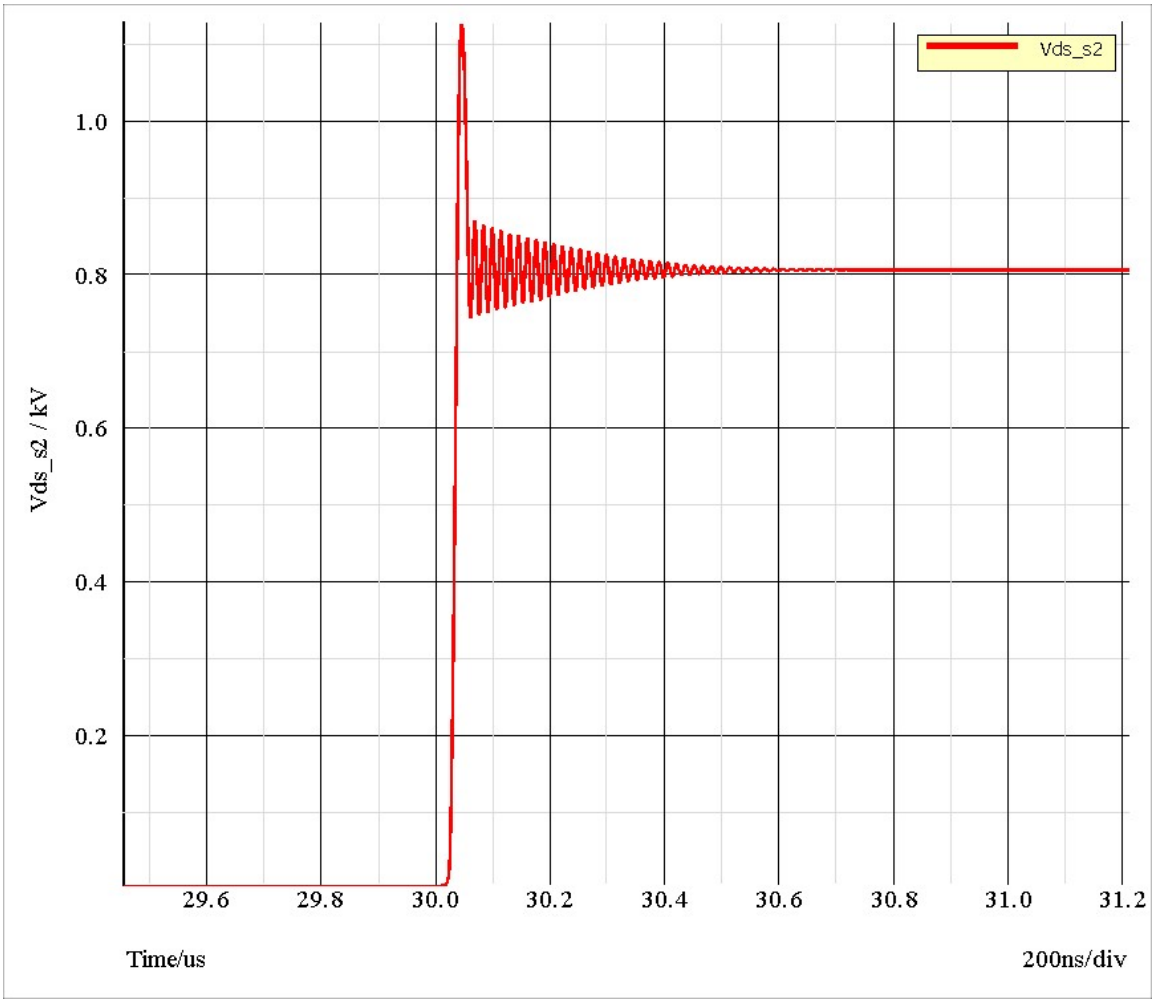


FIGURE B.4.9: Vds Overshoot

Figure B.4.9 depicts the overshoots that occurs. Due to this there are chances of breakdown of the MOSFET. This condition is mitigated in the following way.

B.4.4.1 Working Principle of Overvoltage Clamping

The Overvoltage Clamping mechanism operates by continuously sensing the Vds voltage during switching transitions. When the detected voltage exceeds the predefined clamping threshold, the OVC circuit activates to suppress the overshoot.

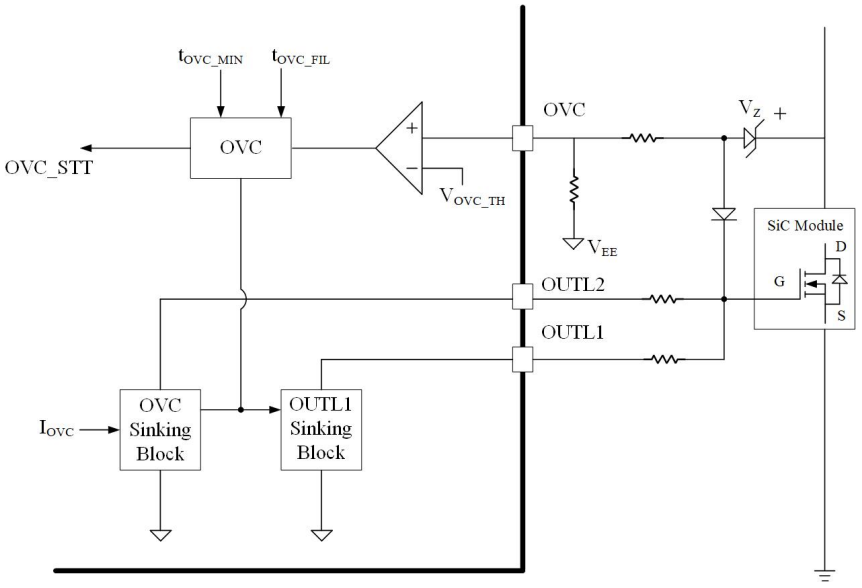


FIGURE B.4.10: Block Diagram of OVC Circuit Reducing Vds Overshoot

Figure B.4.10 illustrates the internal block diagram employed for Overvoltage Clamping (OVC) detection and the subsequent actions. A fast-acting Transient Voltage Suppression (TVS) diode is connected to the OVC pin, which becomes forward-biased when an overvoltage condition is detected. The voltage is then reduced through resistor dividers and fed into the integrated circuit (IC) to the comparator. Appropriate blanking and filtering times are applied to the signal, and the OVC block shifts the sinking current through a current source.

The timing diagram also includes specific intervals designed to prevent false tripping due to erroneous triggers. Filtering time and blanking time helps in preventing false tripping of the feature.

This block diagram provides a comprehensive overview of the OVC detection mechanism, highlighting the role of the TVS diode, resistor dividers, and comparator in

managing overvoltage conditions. The implementation of blanking and filtering times ensures reliable detection and response, enhancing the overall robustness of the system. The voltage overshoot is represented by:

$$V_{ds,overshoot} = L \cdot \frac{di}{dt} \tag{39}$$

where L represents the parasitic inductance and di/dt is the rate of change of current during switching. The clamping circuit effectively limits this overshoot by providing an alternative path for the transient energy, thereby stabilizing the Vds voltage.

B.4.4.2 Timimng Diagram for OVC

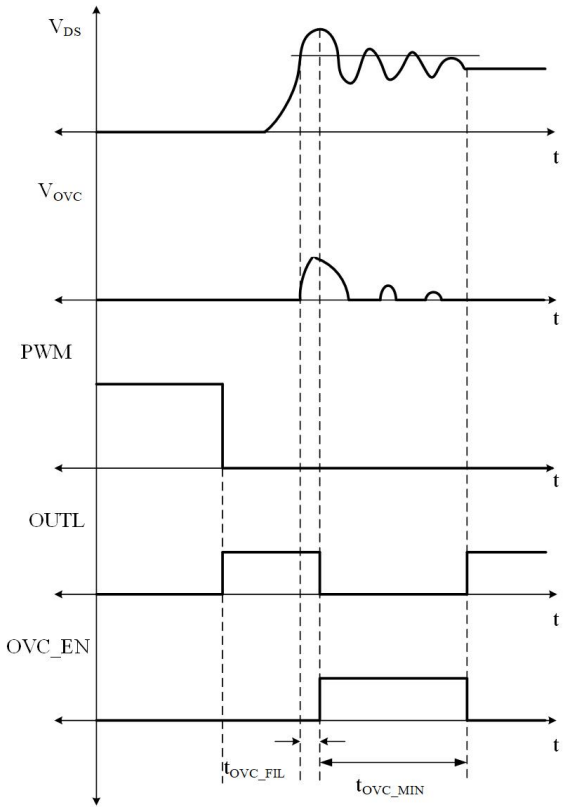


FIGURE B.4.11: Timing Diagram of Overvoltage Clamping during Switching Events

Figure B.4.11 depicts the timing diagram for the OVC operation. When the gate-source voltage V_{gs} exceeds the predefined threshold, the voltage at the OVC pin

proportionally increases. This triggers the deactivation of the MOSFET managing the OUTL path, effectively isolating the standard low-impedance path. Concurrently, a voltage-controlled switch is activated, redirecting the excess current through a programmable current source to ground. This mechanism rapidly mitigates the overvoltage condition, ensuring the voltage is brought back below the critical limit within the defined time frame.

B.4.4.3 Simulation of OVC

Figure B.4.12 illustrates the simulation schematic for the Overvoltage Clamp (OVC) condition, evaluated using the Double Pulse Test (DPT) methodology. The OVC simulation incorporates time-based filtering mechanisms to define the activation duration of the overvoltage protection.

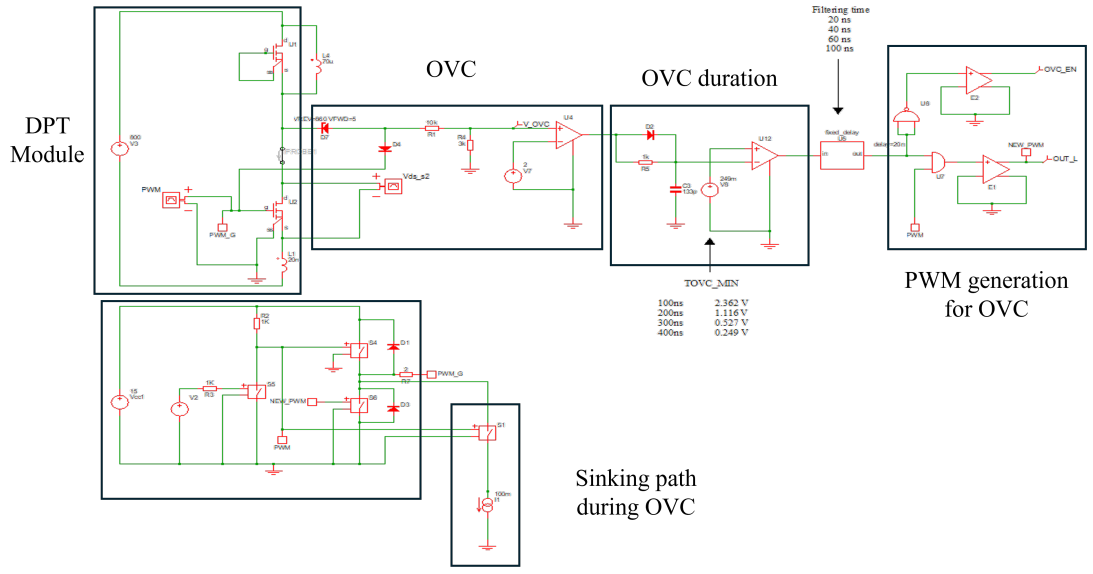


FIGURE B.4.12: Simulation diagram of Overvoltage Clamping (OVC) Circuit

Typically, when the monitored voltage exceeds the predefined threshold for the specified time interval, a low-impedance path is established through the current source to rapidly dissipate excess energy. Following the mitigation of the overvoltage event, the

circuit reverts to the standard OUTL path, ensuring normal operation is restored seamlessly.

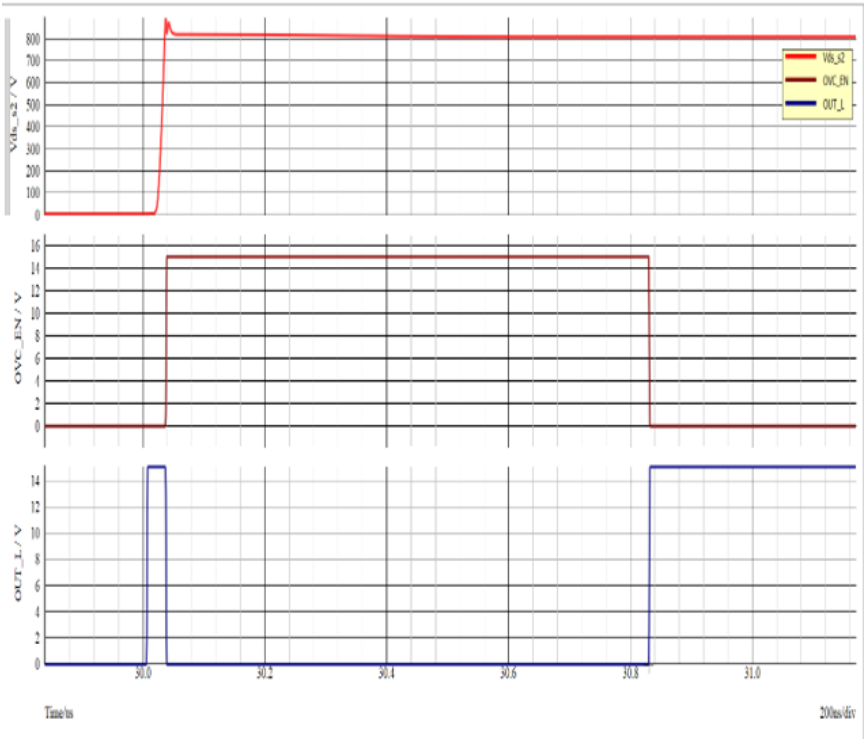


FIGURE B.4.13: Simulation Result for OVC

Figure B.4.13 illustrates the simulation results for the OVC feature. When the drain-source voltage (V_{ds}) exceeds the specified threshold, the voltage-controlled switch is immediately activated, coinciding with the turn-off of the primary MOSFET. This event triggers the current sinking block, which is regulated through PWM control, effectively isolating the standard OUTL path.

During this protective phase, the current source establishes a controlled low-impedance path, allowing excess voltage to be dissipated safely. This operation continues until the V_{ds} is restored to its nominal value, at which point the system reverts to normal operation, indicating successful overvoltage mitigation.

The simulation results confirm the effectiveness of the OVC in managing transient overvoltage conditions, ensuring voltage stability and protecting critical power stage components.

Overvoltage clamping provides a robust method for safeguarding power semiconductors from transient voltage spikes, contributing to the overall reliability and efficiency of traction inverters in electric vehicle applications.

B.4.5 Conclusion

This chapter comprehensively presented the critical protection features integrated into the advanced gate driver, including DESAT protection, Active Miller Clamp (AMC), and Overvoltage Clamp (OVC). An in-depth analysis was conducted for each mechanism, highlighting their operational principles and effectiveness in safeguarding power devices from transient and fault conditions. The detailed exploration of these protection strategies provides a clear understanding of their contributions to enhanced reliability and robustness in high-performance traction inverter. The subsequent chapter introduces the concept of Programmable Soft Turn-Off (PSTO), another pivotal feature of the gate driver, designed to further optimize switching behavior and enhance device protection during critical transitions.

PROGRAMMABLE SOFT TURNING OFF (PSTO)

B.5.1 Introduction to Programmable Soft Turn-Off (PSTO)

Programmable Soft Turn-Off (PSTO) is an advanced protection mechanism implemented in high-power gate drivers for IGBT/MOSFET. In high-voltage applications such as traction inverters and industrial motor drives, switching devices are exposed to severe electrical stress during fault conditions like DESAT and short circuit. Traditional turn-off mechanisms may lead to excessive voltage overshoot and electromagnetic interference (EMI), resulting in potential damage to the power device. PSTO addresses this challenge by utilizing a two-level turn-off mechanism that dynamically adjusts the gate voltage during fault events, thereby reducing voltage transients and mitigating the risk of device failure.

The primary objective of PSTO is to achieve a controlled and gradual reduction in gate voltage when a fault condition is detected. Unlike conventional turn-off, where the gate is pulled down rapidly, PSTO introduces an intermediate voltage step before complete turn-off. This staged approach minimizes the rate of change of voltage (dv/dt) and current (di/dt), effectively lowering switching losses and enhancing device protection. PSTO is particularly advantageous for SiC MOSFETs due to their high switching speeds and lower short-circuit withstand capabilities compared to traditional IGBTs.

B.5.2 Block Diagram for PSTO

Figure B.5.1 illustrates the internal block diagram of the PSTO mechanism. When a fault signal is detected from the DESAT, Overcurrent Protection (OCP), or Short Circuit Protection (SCP), the internal logic of the PSTO initiates **Phase I**. During this phase, the

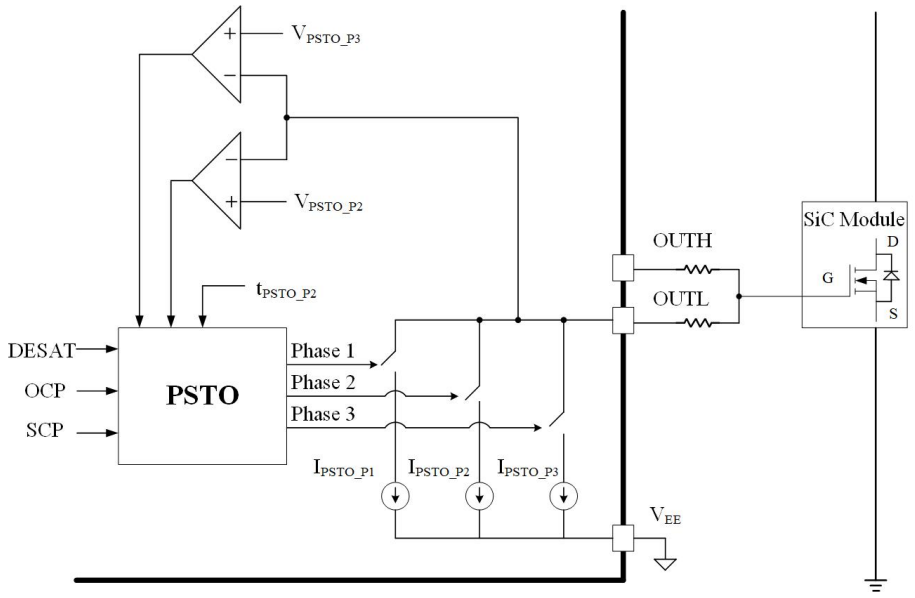


FIGURE B.5.1: Block Diagram for PSTO

gate-source voltage (V_{gs}) is gradually pulled down through a controlled current source to prevent abrupt voltage drops and excessive switching stress.

Upon reaching the predefined programmable voltage level, the system transitions into Phase II, wherein a different current source with a distinct magnitude regulates the gate voltage. Phase II operation can be configured to operate either based on a specified time duration or until a defined voltage threshold is achieved, as illustrated in the block diagram. This phase continues seamlessly until the parameters for entering Phase III are met.

Phase III is activated once the predetermined criteria are satisfied—either the voltage threshold or the time duration is reached. During this phase, the circuit remains in a controlled state until the Active Miller Clamp (AMC) engages, ensuring the gate remains securely off. The block diagram clearly represents the comparators and programmable values associated with each phase transition, providing a structured path for controlled turn-off behavior.

B.5.3 Timing Diagram

Figure B.5.2 illustrates the timing diagram for the PSTO mechanism. The diagram provides a detailed representation of the sequential phases during the PSTO operation. Upon receiving the command signal to initiate the PSTO, the gate-source voltage (V_{gs}) is gradually pulled down through a controlled current source, ensuring a smooth transition. Before each phase begins, a predefined blanking time is introduced. This intentional delay

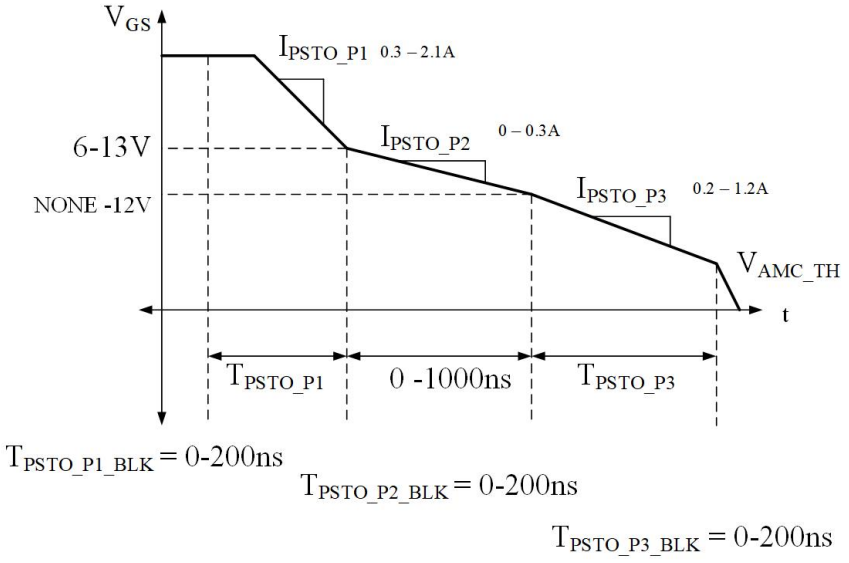


FIGURE B.5.2: Timing Diagram for PSTO

allows for stabilization and prevents premature switching transients. As the voltage level reaches specific thresholds, the PSTO transitions through its distinct phases, ultimately facilitating a smooth turn-off process for the MOSFET or IGBT.

The timing diagram clearly indicates the different programmable voltage levels associated with each phase. Additionally, it highlights the various blanking times, which are configurable through the Graphical User Interface (GUI), enabling fine-tuned control of the turn-off characteristics.

B.5.4 Simulation of PSTO

Figure B.5.3 illustrates the integration architecture of the PSTO mechanism with the OUTH and OUTL stages. The simulation diagram represents the arrangement of three distinct current sources configured to achieve a three-stage turn-off process. When the

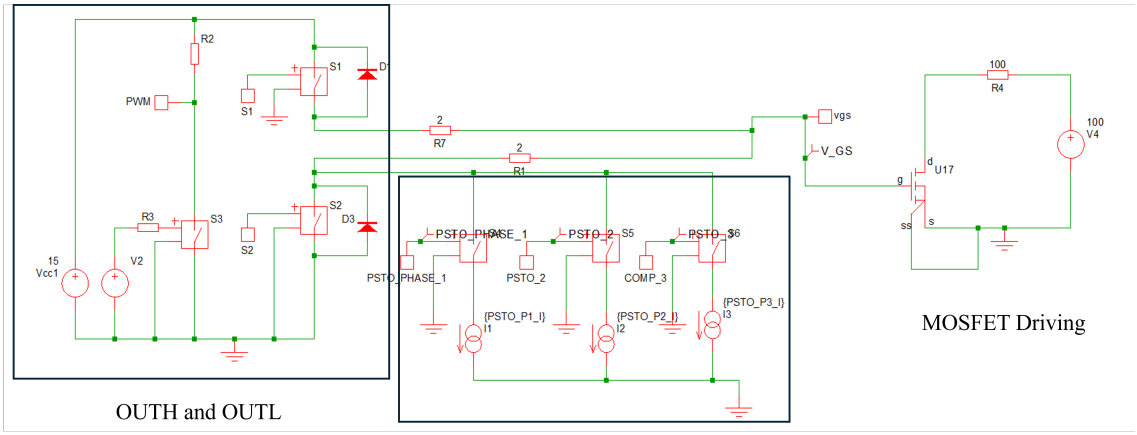


FIGURE B.5.3: Block Diagram of Programmable Soft Turn-Off (PSTO) Circuit

PSTO block is activated, these current sources are sequentially engaged, each corresponding to a specific phase of the turn-off cycle. This staged approach ensures controlled voltage decay and mitigates stress on the power devices, thereby enhancing reliability and reducing overshoot during the transition. This controlled reduction limits the current slope (di/dt) across the MOSFET or IGBT, thereby preventing excessive voltage transients (dv/dt) and mitigating the risk of overshoots.

The diagram clearly depicts the current path and switching sequence, demonstrating the systematic engagement of each current source as the PSTO progresses through its defined stages.

Figure B.5.4 illustrates the mechanism underlying the PSTO turn-on sequence across its distinct operational phases. To emulate a fault condition, a PSTO enable signal is generated and applied to the control logic circuitry. This initiates the sequential activation of PSTO Phase I, Phase II, and Phase III.

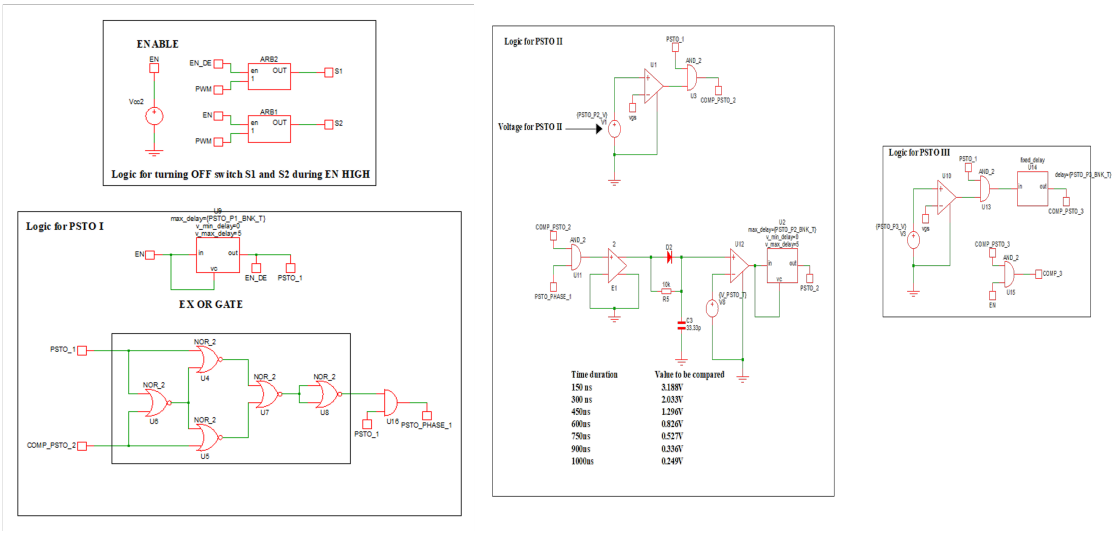


FIGURE B.5.4: Simulation Diagram for PSTO

The transition to Phase II is governed by a predefined voltage threshold, ensuring a smooth progression once the voltage reaches the specified level. Subsequently, Phase III is triggered based on two conditions: either the monitored voltage level falls within the acceptable range, or a predefined time duration elapses, whichever occurs first. This structured mechanism allows the simulation to validate the proper operation of PSTO during fault conditions, ensuring controlled turn-on behavior while preventing voltage spikes and minimizing stress on the power devices.

The operation of the PSTO is further enhanced by employing a **Three-Level Turn-Off Strategy** that modulates the gate voltage through three distinct phases:

- **Phase I: Intermediate Voltage Reduction**

  Upon detection of a fault condition, the gate driver initiates a soft turn-off by gradually reducing the gate voltage to an intermediate level.

- **Phase II: Voltage-Based or Time-Based Transition**

  After reaching the initial intermediate voltage, the system transitions to the second phase, where the gate voltage is further reduced. This phase operates based on either a predefined voltage threshold or a set time duration, ensuring a controlled descent. This programmable flexibility allows designers to optimize the turn-off process according to application-specific requirements.

- **Phase III: Final Turn-Off Stage**

  Once the specified voltage or time criteria are met, the circuit progresses to the final turn-off stage. During this phase, the gate voltage is completely driven to the OFF state, ensuring the MOSFET or IGBT is securely deactivated. This step not only minimizes residual energy in parasitic inductances but also reduces the possibility of voltage overshoot and EMI generation. In this stage the AMC also enables bringing the V_{gs} to the VEE level.

The three-level turn-off mechanism integrated within the PSTO provides enhanced reliability and robustness during fault events by ensuring smooth voltage transitions, minimizing electrical stress, and extending the operational lifespan of the power device. The simulation results validate the effectiveness of this multi-stage turn-off process in achieving stable operation during critical conditions.

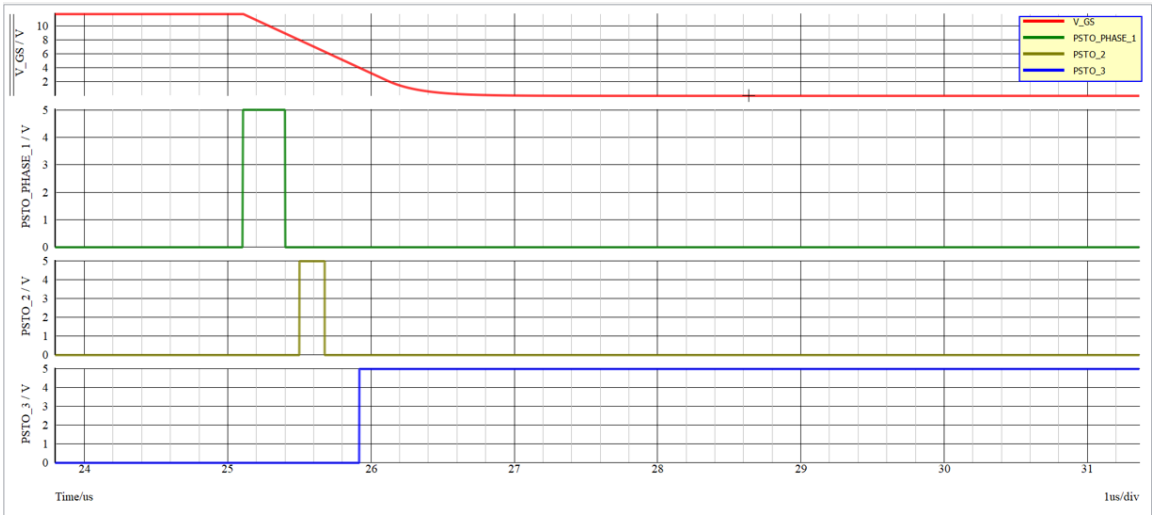


FIGURE B.5.5: Simulation Result for PSTO

Figure B.5.5 presents the simulation results for the Programmable Soft Turn-Off (PSTO) mechanism. Upon receiving the enable command, the PSTO logic initiates the turn-off sequence, adhering to the defined timing configurations. This results in the controlled reduction of the gate-source voltage (V_{gs}), as depicted in the simulation waveforms.

The simulation output distinctly demonstrates the activation of the three phases of PSTO, each contributing to a smooth and gradual voltage transition. In Phase I, the gate voltage is pulled down to an intermediate level, ensuring that voltage transients are minimized. This is followed by Phase II, where the voltage is further reduced based on a predefined threshold or time delay. Finally, Phase III completes the turn-off process by fully deactivating the gate voltage, ensuring the MOSFET or IGBT is securely turned off.

The results validate the effectiveness of the three-level turn-off strategy, showcasing its capability to minimize voltage overshoot and suppress transient spikes during fault conditions.

B.5.5 Conclusion

The integration of the PSTO mechanism in traction inverters and industrial motor drives represents a significant advancement in power electronics protection strategies. By employing a structured, multi-phase voltage reduction process, the PSTO effectively mitigates transient spikes and reduces the risk of voltage overshoot during turn-off events. This controlled shutdown minimizes electrical stress on power devices, extending their operational lifespan and enhancing overall system reliability.

The three-level turn-off strategy of the PSTO ensures that voltage transitions are smooth and well-regulated, preventing abrupt changes that could lead to catastrophic device failure. Furthermore, the programmable nature of each phase provides design flexibility, enabling engineers to fine-tune protection parameters according to specific application requirements.

The simulation results validate the robustness of the PSTO mechanism, demonstrating its capability to maintain voltage stability and suppress transients effectively. Its application in high-performance motor drives and traction inverters not only safeguards critical components but also improves reliability.

UVLO AND OVLO, OCP AND SCP

B.6.1 Introduction

In the field of electric mobility, traction inverters play a pivotal role in the efficient and reliable conversion of electrical energy to drive electric motors. Given the high voltage and current stresses encountered during operation, robust protection mechanisms are critical to ensure system stability and prevent catastrophic failures. This chapter provides an in-depth exploration of four essential protection features integrated into gate drivers for traction inverter applications: **Undervoltage Lockout (UVLO)**, **Overvoltage Lockout (OVLO)**, **Overcurrent Protection (OCP)**, and **Short Circuit Protection (SCP)**.

In traction inverters, Undervoltage Lockout (UVLO) is a crucial safety feature that monitors the supply voltage levels on both the primary and secondary sides, specifically V_{CC} and V_{DD}. During electric vehicle acceleration or regenerative braking, fluctuations in the supply voltage are common. UVLO ensures that the gate driver remains disabled if the voltage drops below a predefined threshold, thereby preventing the IGBTs or SiC MOSFETs from operating under unstable or unsafe conditions. This is vital for maintaining the integrity of the power stage, as insufficient drive voltage can result in increased conduction losses and partial saturation, which may lead to device overheating and premature failure.

Overvoltage Lockout (OVLO) complements UVLO by providing protection against excessive voltage levels that can arise from regenerative braking or grid fluctuations. In high-power traction inverters, voltage surges can exceed the maximum ratings of power devices, potentially causing gate oxide breakdown and long-term reliability issues. OVLO continuously monitors the secondary-side supply, V_{DD}, and compares it against a fixed reference voltage. If the monitored voltage exceeds the threshold, the driver is immediately disabled to prevent damage. This mechanism protects both the driver IC and

power switch from electrical overstress, ensuring reliable operation even under harsh transient conditions.

To further safeguard the traction inverter, Overcurrent Protection (OCP) is implemented to monitor the current flowing through the power switches. During conditions such as motor stall, excessive torque demand, or sudden load changes, current surges are likely to occur. OCP detects these anomalies and triggers an immediate shutdown of the gate driver when the current exceeds a predefined limit. This rapid intervention prevents thermal stress, mitigates the risk of junction overheating, and protects the inverter's semiconductor devices from permanent damage.

Short Circuit Protection (SCP) is another vital mechanism designed to detect short circuit events within the inverter circuitry. In applications like electric vehicles, short circuits can result from wiring faults, component failures, or insulation breakdowns. SCP instantly deactivates the gate driver upon detection of a short circuit, preventing excessive fault currents from damaging the MOSFETs or IGBTs. This fast-acting response is crucial for maintaining the reliability and safety of the traction inverter during fault conditions.

Collectively, the integration of UVLO, OVLO, OCP, and SCP in traction inverter gate drivers forms a comprehensive protective framework. These mechanisms not only enhance the reliability and lifespan of power devices but also contribute to the overall efficiency and robustness of electric vehicle powertrains. In the subsequent sections, each of these protection strategies is analyzed in detail, emphasizing their design considerations, operational principles, and impact on inverter performance.

B.6.2 Overcurrent Protection (OCP)

To ensure the reliability and safety of power electronic devices, Overcurrent Protection (OCP) and Short Circuit Protection (SCP) are implemented to safeguard MOSFETs and IGBTs from catastrophic breakdown during fault conditions. Both mechanisms operate

by monitoring the voltage at the ISEN pin, which serves as the non-inverting input to the protection comparators.

OCP is activated when the voltage at the ISEN pin surpasses a predefined threshold for a duration exceeding the specified filtering time, following the expiration of a blanking period. The blanking time is crucial for preventing false triggering during the initial turn-on transitions of the power switch. Upon detection of an overcurrent event, the OCP logic initiates a controlled shutdown of the power switch, with the total delay encompassing a fixed 150 ns propagation time in addition to the comparator's filtering time.

Similarly, SCP follows the same detection principle, where a surge in current that exceeds the threshold triggers the protection mechanism. The filtering and blanking times are designed to avoid spurious activations, ensuring that only legitimate fault events result in driver shutdown. The controlled turn-off minimizes stress on the power switch, preventing device failure and enhancing overall system reliability.

Together, OCP and SCP form a robust protective framework for high-power applications, effectively preventing damage to switching devices during abnormal current conditions [112, 122].

B.6.3 Block Diagram for OCP and SCP

Figure B.6.1 illustrates the internal block diagram of the Overcurrent Protection (OCP) and Short Circuit Protection (SCP) mechanisms. The system is equipped with a current sense pin that monitors the current flowing through the IGBT or MOSFET module. This current is accurately sensed and converted into a proportional voltage signal, which is then fed to the control IC.

To prevent false triggering during transient conditions, a predefined blanking time is applied to the sensed signal. This ensures that minor fluctuations do not activate the protection prematurely. After the blanking interval, the voltage signal is processed by comparators that evaluate it against predefined threshold levels. If the sensed voltage

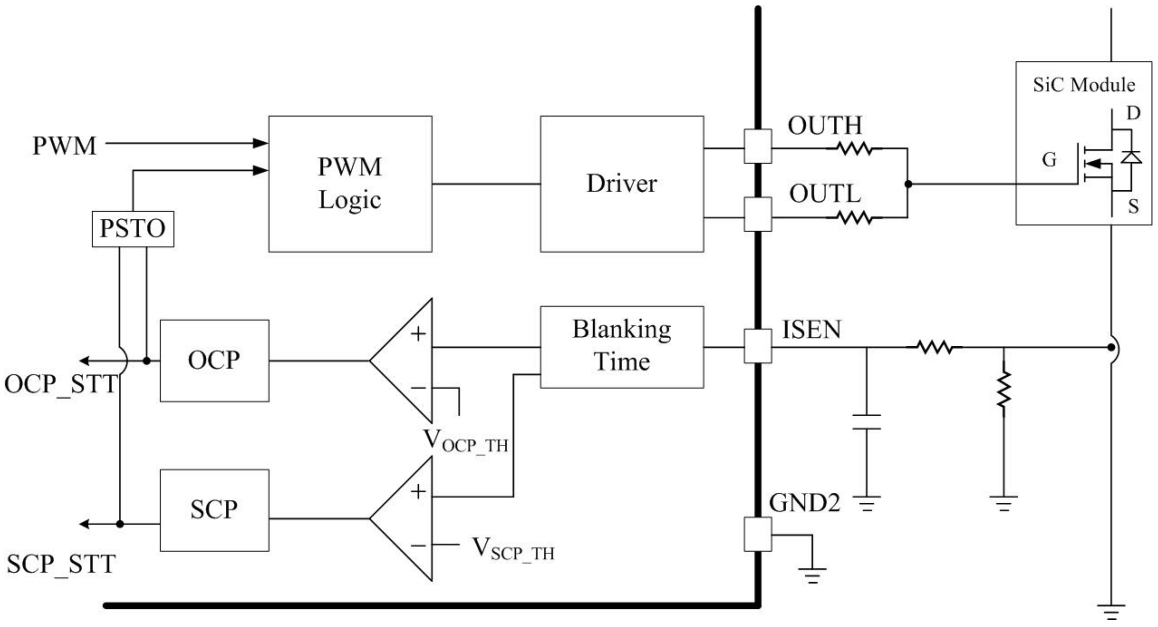


FIGURE B.6.1: Block Diagram of OCP SCP

exceeds the set threshold, the OCP and SCP logic blocks are activated, signaling a fault condition.

Upon detecting an overcurrent or short circuit event, the protection logic initiates the Programmable Soft Turn-Off (PSTO) mechanism. This staged shutdown sequence ensures a controlled turn-off of the power switch, minimizing voltage transients and safeguarding the device from damage.

B.6.3.1 Simulation of OCP and SCP

Figure B.6.2 presents the simulation schematic for the OCP and SCP mechanisms. To emulate fault conditions, a DPT is performed, allowing the circuit to simulate transient current spikes commonly observed during switching events.

The design incorporates an RC filter to prevent false triggering of the protection circuitry. During turn-off transitions, rapid current variations often generate spikes that could erroneously activate the OCP or SCP logic. The RC filter effectively attenuates these transient disturbances, ensuring only legitimate overcurrent or short circuit events are detected.

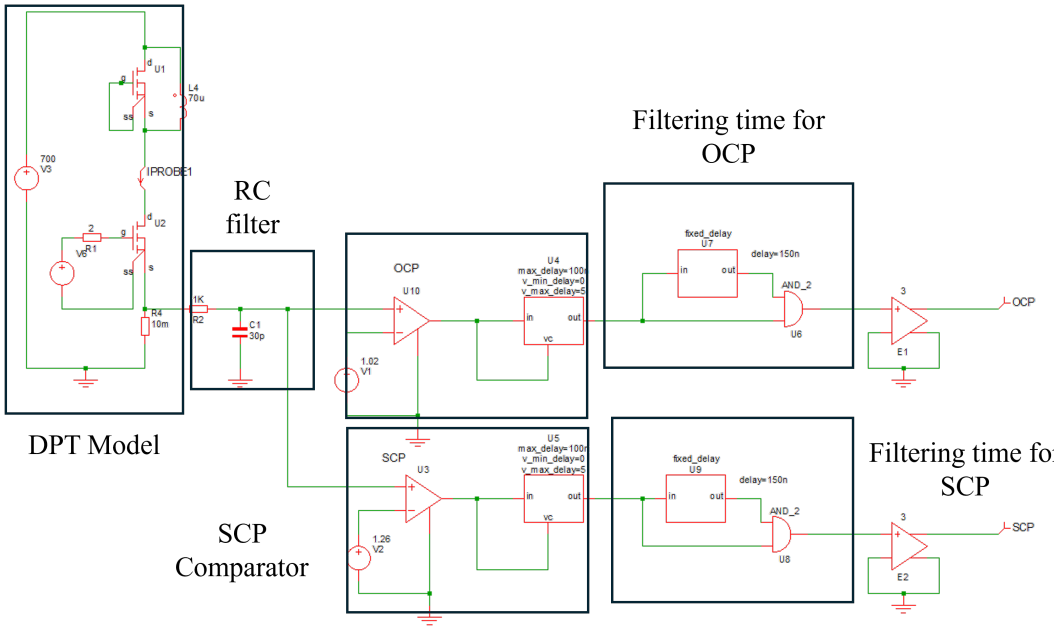


FIGURE B.6.2: Simulation Diagram for OCP and SCP

The filtered signal is then processed by comparators that evaluate the voltage against predefined threshold levels. Upon detection of a fault, the comparator outputs a fault signal, which is subsequently relayed to the Programmable Soft Turn-Off (PSTO) block. This initiates a controlled reduction of the gate-source voltage (V_{gs}), facilitating a smooth and reliable turn-off of the power device, thereby preventing damage and enhancing system stability.

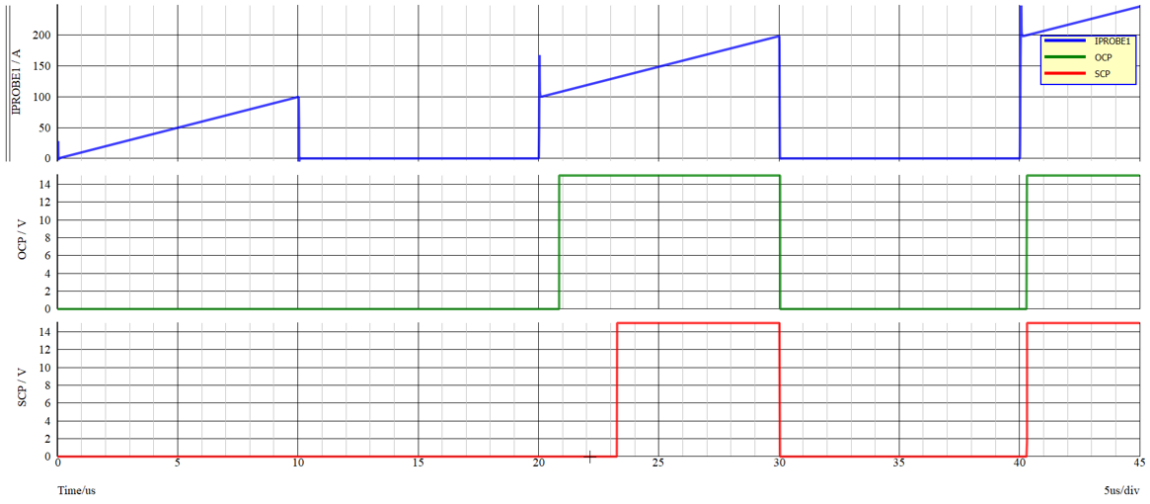


FIGURE B.6.3: Output of OCP and SCP

Figure B.6.3 illustrates the simulation results for the OCP and SCP mechanisms during a DPT. The simulation demonstrates the activation sequence, where the OCP is triggered as soon as the sensed current exceeds the predefined threshold limit. This immediate response prevents excessive current from causing thermal stress and potential damage to the power device.

As the current continues to rise beyond the OCP limit, the SCP mechanism is subsequently activated. This secondary layer of protection is designed to detect critical overcurrent conditions that surpass the initial OCP threshold, ensuring comprehensive safeguarding of the power stage.

Upon detection of either OCP or SCP, the Programmable Soft Turn-Off (PSTO) mechanism is immediately engaged. This action initiates a controlled reduction of the gate-source voltage (V_{gs}), smoothly deactivating the MOSFET or IGBT to prevent electrical overstress and maintain system reliability.

B.6.4 UVLO and OVLO

Figure B.6.4 illustrates the simulation implementation of the Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) mechanisms. The design incorporates a comparator that continuously monitors the voltage levels and compares them against a predefined reference value, which is programmable through the Graphical User Interface (GUI). This reference value is configured based on specific design parameters of the gate driver to ensure that the operating conditions remain within safe margins.

To enhance reliability and prevent false triggering during transient fluctuations, a filtering time is introduced. This delay mechanism effectively filters out momentary voltage dips or surges, preventing erroneous activation of the protection circuitry. This ensures that minor transients do not disrupt normal operation while maintaining system stability.

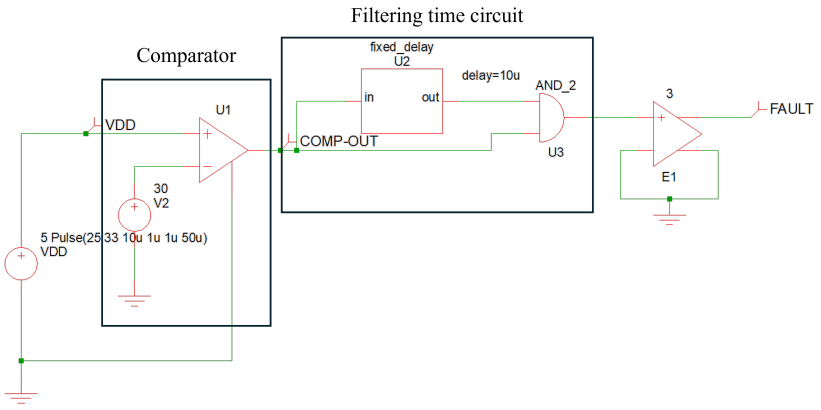


FIGURE B.6.4: Simulation Diagram for UVLO and OVLO

Upon detection of a fault condition—either an undervoltage or overvoltage event—the comparator output triggers the protection mechanism, resulting in the immediate shutdown of the Pulse Width Modulation (PWM) signal. This rapid response prevents the power device from operating under unsafe voltage conditions, thereby safeguarding both the driver and the power stage from potential damage.

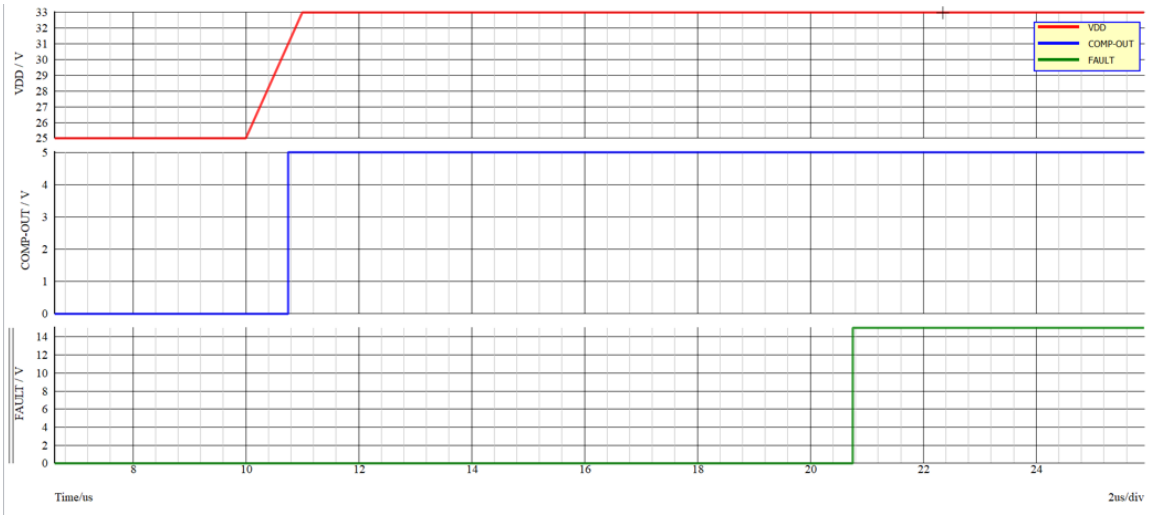


FIGURE B.6.5: Simulation Result for UVLO and OVLO

Figure B.6.5 presents the simulation results for the Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) mechanisms. The results illustrate the fault detection process initiated when the monitored voltage exceeds or falls below the predefined threshold. The comparator output transitions to a high state as soon as the voltage surpasses the configured limit, indicating a fault condition.

To enhance stability and prevent false triggering, an appropriate hysteresis is incorporated into the comparator design. This hysteresis band allows the circuit to tolerate minor voltage fluctuations without prematurely activating the protection mechanism. Additionally, a deliberate delay is introduced before the fault signal is asserted. This delay ensures that transient disturbances are filtered out, thus preventing unnecessary fault triggering and enhancing system reliability.

The simulation results validate the effectiveness of the UVLO and OVLO implementations, confirming their capability to reliably detect fault conditions while minimizing false positives.

B.6.5 Conclusion

The integration of OCP, SCP, OVLO, and UVLO mechanisms within gate driver circuits significantly enhances the reliability and safety of power electronic systems, particularly in high-power applications such as traction inverters and industrial motor drives. OCP and SCP provide robust protection against excessive current conditions, mitigating the risk of thermal stress and device failure. These mechanisms are designed to respond rapidly to overcurrent events, triggering the PSTO to ensure smooth and controlled turn-off of the power switch, thereby preventing catastrophic breakdown.

Similarly, OVLO and UVLO safeguard the system from voltage anomalies by monitoring supply levels and disengaging the driver during unsafe conditions. OVLO effectively prevents damage due to overvoltage events, while UVLO ensures stable operation by disabling the gate driver during insufficient supply voltages. Together, these protective features form a comprehensive framework that maintains the integrity of power devices, extends operational lifespan, and enhances overall system resilience.

The simulation results validate the effectiveness of these protection mechanisms, confirming their capability to detect and respond to fault conditions promptly. This

layered approach to protection not only prevents device damage but also contributes to the safe and reliable operation of power converters in demanding applications.

TESTING OF GATE DRIVER

B.7.1 Introduction

The development of high-performance traction inverters necessitates rigorous testing and evaluation of gate driver functionalities to ensure reliability and efficiency under various operating conditions. To achieve this, a dedicated evaluation board has been designed to validate the critical protection and switching features of the traction inverter-based gate driver.

The evaluation board is equipped to conduct Double Pulse Testing (DPT), which is an industry-standard method for characterizing the dynamic performance of power devices. Through DPT, the gate-source voltage (V_{gs}) is monitored with respect to the IN+ signal to evaluate switching behavior, gate drive strength, and transient responses during high-speed operation. This testing approach provides critical insights into voltage overshoot, switching losses, and turn-off characteristics.

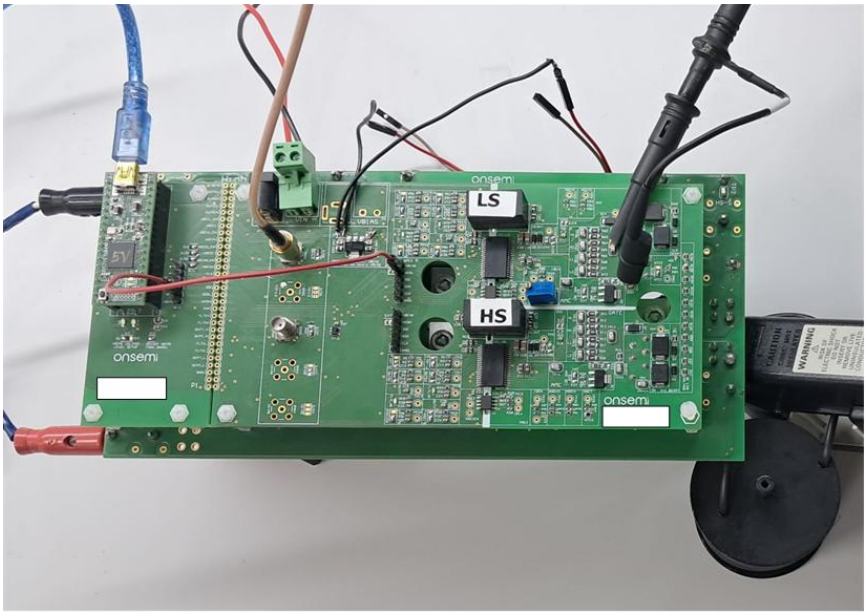


FIGURE B.7.1: Actual Photograph of Evaluation board

Figure B.7.1 shows the acutal photograph of the evaluation board. Additionally, the evaluation platform allows for detailed observation of the DESAT protection mechanism. DESAT detection is crucial for identifying overcurrent events that may lead to device failure if not mitigated promptly. By integrating this feature into the evaluation board, the system's ability to trigger protective responses under fault conditions can be thoroughly analyzed.

This chapter provides a detailed overview of the evaluation board's design, its functional blocks, and the testing methodology employed to validate the gate driver's performance. Key results from DPT, V_{gs} monitoring, and DESAT evaluation are presented to demonstrate the board's effectiveness in safeguarding traction inverter applications.

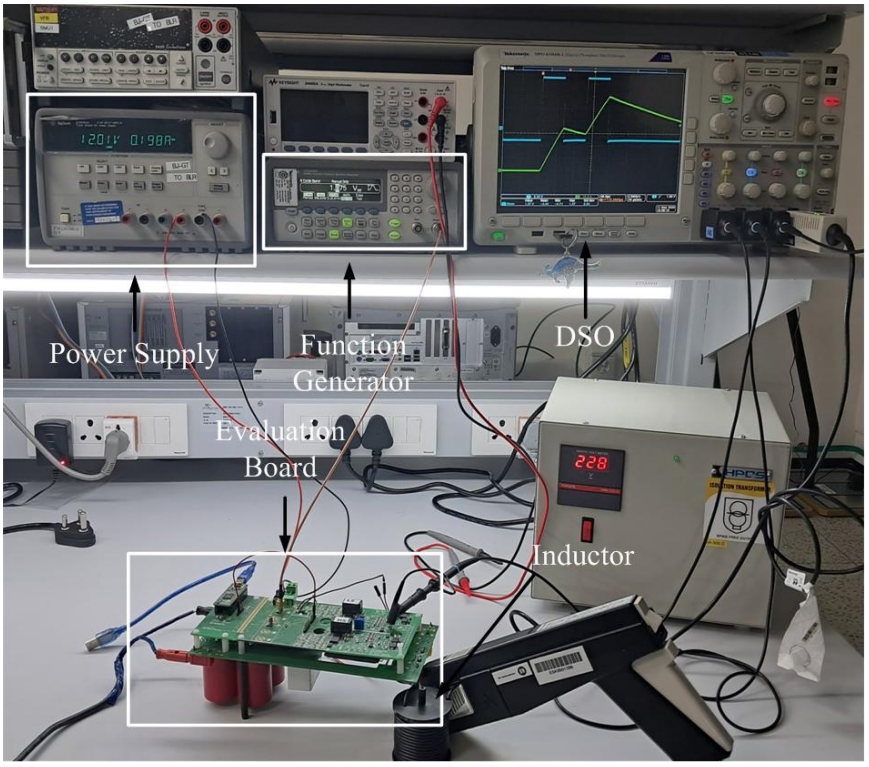


FIGURE B.7.2: Setup for Checking Functionalities

Figure B.7.2 illustrates the complete experimental setup designed to evaluate the performance of the gate driver IC. The setup comprises a function generator, a Graphical User Interface (GUI), a current measurement probe, and an oscilloscope.

The function generator provides the necessary input signals to the gate driver, enabling controlled testing of switching characteristics and protection mechanisms. The GUI facilitates real-time monitoring and parameter adjustments, allowing fine-tuned control of the gate driver's operating conditions.

Current measurements are captured using a high-precision current probe, which is connected to the oscilloscope for accurate waveform visualization. This configuration allows for the detailed observation of gate-source voltage (V_{gs}), inductor currents, and transient responses during switching events.

The experimental setup effectively validates the functionality and reliability of the gate driver IC under various test conditions, ensuring its suitability for high-performance traction inverter applications.

B.7.2 Double Pulse Test

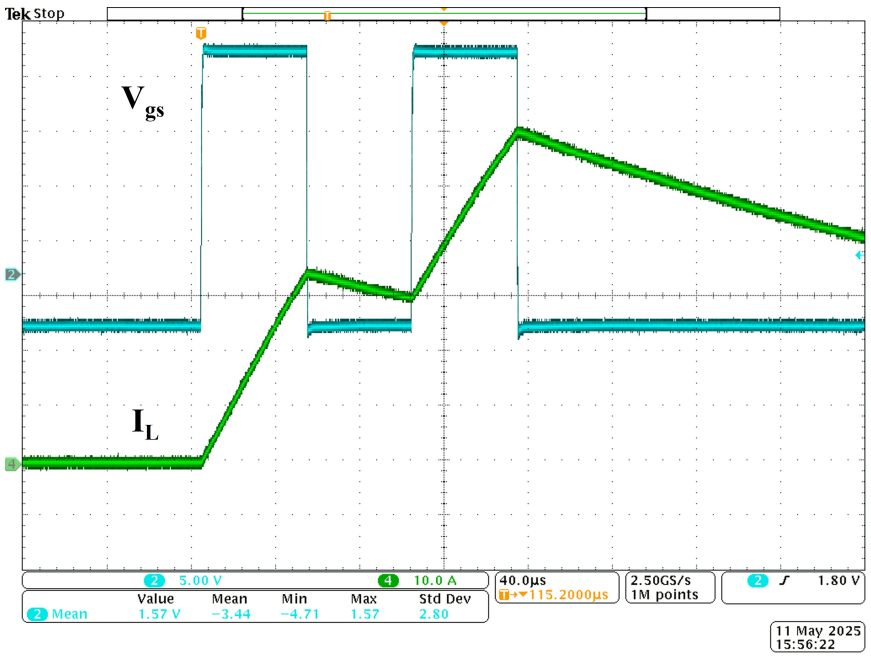


FIGURE B.7.3: Dual Pulse Test Result

A Double Pulse Test (DPT) was conducted on the MOSFET module to evaluate its switching characteristics and verify the gate driver functionalities. Figure B.7.3 illustrates

the test results, showcasing the gate-source voltage (V_{gs}) transition from +20 V to -5 V during the switching operation. This controlled transition highlights the effective management of gate drive signals, ensuring proper switching behavior.

Additionally, the waveform also depicts the inductor current rise during the MOSFET's turn-on phase. The smooth current ramp indicates efficient energy transfer and minimal switching losses, validating the reliability of the gate driver during high-speed operation.

The DPT analysis confirms the gate driver's capability to handle rapid voltage transitions and current surges, reinforcing its suitability for traction inverter applications.

B.7.3 OUT Drive Test

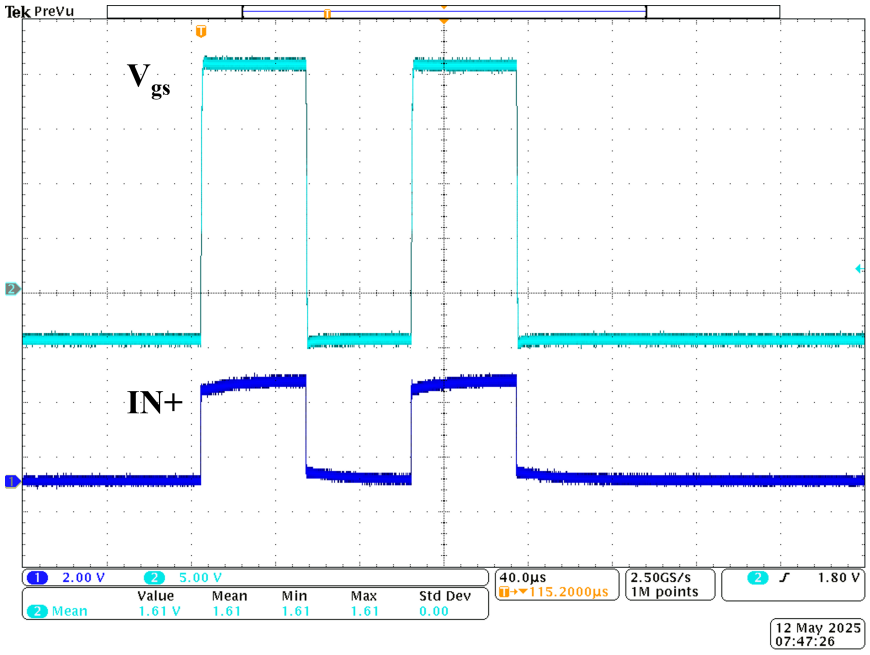


FIGURE B.7.4: Vgs Generated for MOSFET

Figure B.7.4 illustrates the relationship between the IN+ signal and the gate-source voltage (V_{gs}) during the Double Pulse Test (DPT) for the MOSFET module. In this configuration, the IN+ signal is supplied through a function generator, directly driving the gate voltage. The V_{gs} waveform effectively mirrors the IN+ input, ensuring synchronized switching action.

It is important to note that the IN- signal is not utilized during DPT testing. IN- is primarily used when both sides of the gate driver are active simultaneously, which is not required in single-sided evaluations like the DPT. The isolated control of IN+ simplifies the test setup and enables precise monitoring of V_{gs} behavior.

This setup validates the gate driver's capability to follow the IN+ command accurately, ensuring reliable switching and minimal delay during high-frequency operations.

B.7.4 Hardware Validation of DESAT Operation

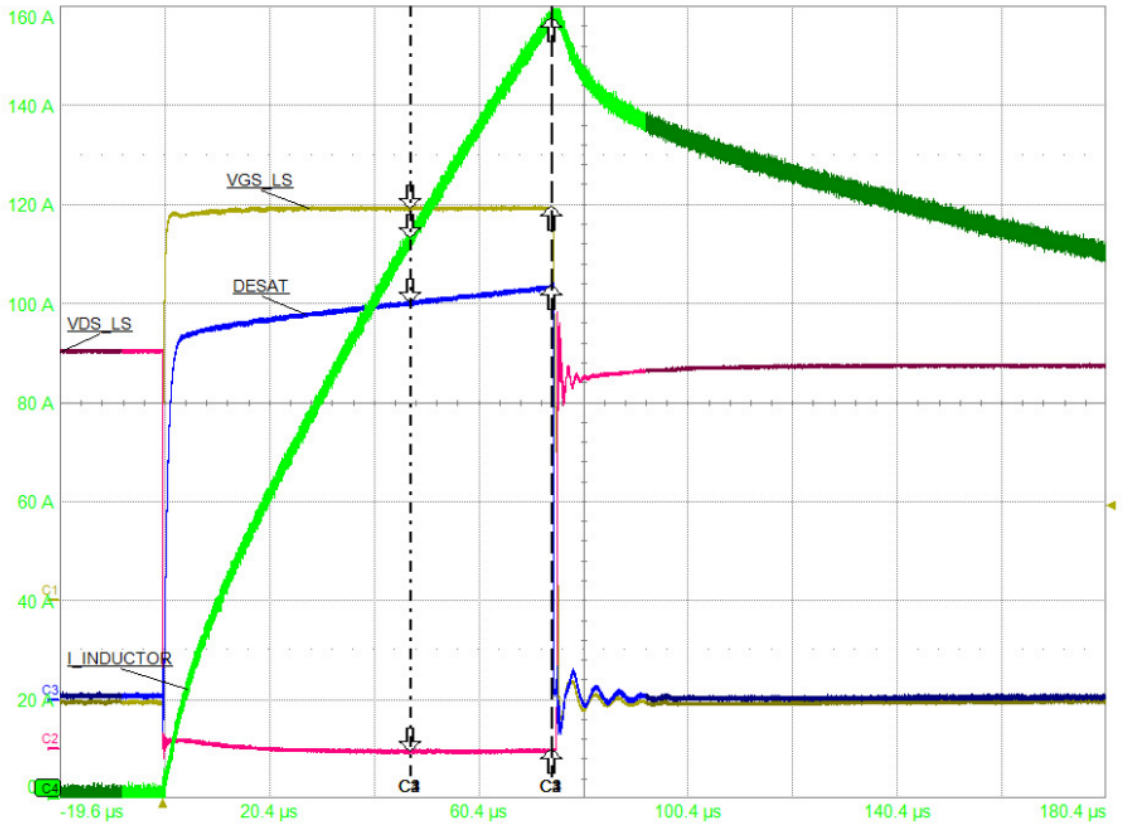


FIGURE B.7.5: Hardware Result for DESAT

Figure B.7.5 presents the actual hardware results obtained during the DESAT operation. In this test, a single pulse is applied to trigger the DESAT protection mechanism. The results clearly demonstrate that as soon as the current reaches the predefined threshold, the DESAT circuitry activates, sending a command to the

Programmable Soft Turn-Off (PSTO). This action initiates an immediate shutdown of the power switch, causing the inductor current to be rapidly clamped.

This hardware validation confirms the effectiveness of the DESAT mechanism in real-world conditions, mirroring the behavior observed during simulation. The prompt response to overcurrent conditions highlights the reliability of DESAT protection in preventing damage to the power stage, thereby ensuring the safe operation of the gate driver and associated MOSFET or IGBT.

B.7.5 Conclusion

The evaluation of protection mechanisms in traction inverter-based gate drivers, including UVLO, OVLO, OCP, SCP, and DESAT, demonstrated effective fault detection and reliable turn-off strategies during simulation analysis. These simulation studies validated the robustness of each mechanism in preventing voltage and current anomalies, ensuring the stability and protection of power devices.

To further confirm the reliability of these protective features, hardware-based testing was conducted using a dedicated evaluation board. The experimental results closely matched the simulation outcomes, providing empirical evidence of the system's capability to respond promptly to overvoltage, undervoltage, overcurrent, and short circuit events. Key tests, including Double Pulse Testing (DPT) for V_{gs} analysis and DESAT operation, highlighted the gate driver's ability to safeguard the power stage with precision and minimal delay.

The consistency between simulation and hardware results reinforces the effectiveness of the proposed gate driver design for traction inverter applications. This dual-layer validation not only underscores the reliability of the protection mechanisms but also establishes a solid foundation for the deployment of these technologies in high-performance power electronics.

CONCLUSION AND FUTURE SCOPE

B.8.1 Conclusion

This thesis presented the comprehensive design, simulation, and hardware validation of a gate driver features specifically optimized for traction inverter applications. The development process encompassed the implementation of critical protection mechanisms, including Undervoltage Lockout (UVLO), Overvoltage Lockout (OVLO), Overcurrent Protection (OCP), Short Circuit Protection (SCP), and DESAT detection. These functionalities were rigorously tested through both simulation analysis and real-world hardware evaluation to ensure reliability and robustness under varying operational conditions.

The simulation results demonstrated effective fault detection, reliable switching control, and smooth turn-off transitions during voltage and current anomalies. Key tests, such as DPT, confirmed the gate driver's capability to handle rapid switching events, maintain stable V_{gs} behavior, and prevent damage to power devices during transient conditions. Furthermore, the hardware implementation on the evaluation board validated the simulation findings, showcasing the successful operation of protection circuits and smooth integration of the Programmable Soft Turn-Off (PSTO) mechanism.

The seamless correlation between simulation and hardware results underscores the reliability of the proposed gate driver design, affirming its suitability for high-performance traction inverter applications. All functionalities performed as expected, ensuring protection and stable operation during critical switching events.

B.8.2 Future Scope

The next phase of this research involves deploying the developed gate driver into an actual traction inverter system to analyze its performance under real-world operating conditions. Parameters such as long-term reliability, and efficiency in high-power scenarios can be further explored. Additionally, the integration of advanced communication protocols and adaptive control techniques could enhance system responsiveness and energy optimization in electric vehicle applications.

The successful simulation and hardware validation presented in this work establish a solid foundation for future deployment in electric mobility, contributing to the advancement of efficient and reliable traction inverter technologies.

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